Development of Fast-Switching SiC Transistor

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Recently, with the growing global interest on energy saving, power device efficiency is becoming increasingly important. Almost all power devices are fabricated utilizing silicon (Si) and their performances have approached to the limit that can be obtained from Si. Silicon carbide (SiC) is one of the candidate materials for innovative power devices that can replace Si devices. The authors have developed a reduced surface field (RESURF) type junction field effect transistor (JFET) as the new power switching device with low-on-resistance and fast-switching characteristics that takes full advantage of SiC. This paper provides an overview of the design, fabricating process and electrical properties of this RESURF-JFET and also the characteristics enhanced by microfabrication. The fabricated 400 V /2.5 A RESURF-JFET shows a low specific on-resistance of 5.2 mWcm2 and a fast switching speed of less than 10 ns. These characteristics are superior to those of Si MOSFETs of the similar current and blocking voltage. These results show that the application of the SiC RESURF-JFET to power electronics will provide significant benefits in improving efficiency, dynamic performance and compactness.

1. Introduction

1-1 Features of SiC and background of device development

Recently, due to the growing global interest in energy saving, efficiency is becoming more important in power devices. Therefore, it is very important to develop power devices that have lower loss and higher efficiency. Almost all power devices are fabricated using silicon (Si), but their performances have approached the theoretical limits of Si power device.

It is necessary to put semiconductors having better properties than Si in practical use. Silicon carbide (SiC) is one of the candidates for the semiconductor material for innovative power devices that will replace Si devices [(1), (2)].

The unique features of SiC are that it occurs in many crystalline polytypes although it is constant in composition, and that each polytype has different characteristics. Among the various crystalline polytypes of SiC, 4H-SiC is most promising as a semiconductor material for power devices. Compared to Si, 4H-SiC has a bandgap about 3 times wider and an electric breakdown field about 10 times larger. This means that in SiC devices, the distance of drift region, which is depleted during the blocking mode, can be reduced to about one-tenth of that of Si devices having the same blocking voltage. Moreover, in SiC devices, the dopant concentration in drift region can be about 100 times higher compared to Si devices. The majority of the on-resistance of a power device having a high blocking voltage is drift region resistance. Therefore, the on-resistance of SiC power devices can be about a thousandth that of Si power devices having the same blocking voltage. The saturated electron drift velocity of 4H-SiC is about twice as fast as that of Si. In addition, the drift distance of 4H-SiC power devices can be made shorter than that of Si ones having the same blocking voltage. These properties indicate that SiC switching power devices can be made faster than Si switching power devices. Furthermore, the thermal conductivity of 4H-SiC is about three times that of Si. This indicates that in addition to having the three times wider bandgap and higher intrinsic semiconductor temperature, SiC power devices can be stable at higher temperatures compared to Si devices.

As is stated above, SiC power devices are expected to be superior to Si power devices in terms of low-loss operation, fast switching time and high temperature operation stability. These are the characteristics required for new-generation power devices

Sumitomo Electric is developing various types of SiC devices such as reduced surface field (RESURF) type junction field effect transistor (JFET) and metal/oxide/semiconductor field effect transistor (MOSFET) for switching power supplies and automotive power electronics. In the previous paper the authors described the operation principles, fabrication process and characteristics of the RESURF-type SiC JFET (hereinafter referred to as SiC RESURF-JFET) that they had developed [(3)]. The authors have worked on miniaturizing device size and successfully developed a low-on-resistance, high-current and fast-switching SiC RESURF-JFET. This paper provides an overview of this SiC RESURF-JFET's design, fabrication process, electrical properties and switching characteristics.

2. Design and fabrication process of RESURF-JFET

2-1 Features of RESURF-JFET

Figure 1 shows the cross-sectional view of a RESURF-JFET of typical size and dopant concentration.

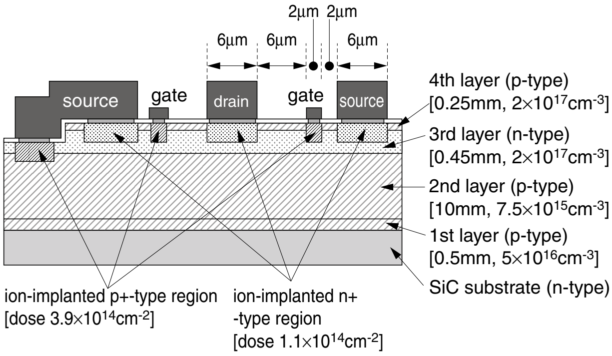

Fig. 1. Cross-sectional view of RESURF-JFET

The typical thickness and dopant concentration of each layer and the distances between electrodes are shown in the figure. The device consists of four epitaxial layers and has a double-RESURF structure between the drain and gate electrodes. **Figure 2** shows the formation of depletion layer and the distribution of electric field in the gate-drain area for the JFETs with and without a RESURF structure.

The depletion layer of a RESURF-JFET extends vertically at the drift region between the gate and the drain when the transistor is off. The electric field strength in drift region is almost uniform, and the concentration of electric field around the gate electrode is reduced. Therefore, the RESURF structure suppresses the occurrence of breakdown caused by field concentration, and improves the blocking characteristics of the device. In other words, the average electric field in the drift region of a RESURF-JFET can be designed to be higher. This means that a RESURF-type JFET has a shorter drift region and a lower on-resistance than the one without a RESURF structure that has the same blocking voltage. Furthermore, in the drift region of a RESURF structure, the distribution of electric field strength is independent of dopant concentration. Therefore, the dopant concentration of a RESURF-JFET can be made higher so that its on-resistance can be made lower.

As mentioned above, a SiC RESURF-JFET is advantageous in that it has both a high blocking voltage and a low on-resistance and makes the most of the properties of SiC.

2-2 Design

Miniaturization is very effective in enhancing device characteristics, including low on-resistance and fast switching. In this paper the authors report on the two types of devices that can be used in comparative evaluation. **Figure 3** shows the cross-sectional views of the two types of devices. One is device B (the lower figure in **Fig. 3**), which is fabricated on a 3×3 mm chip. The other is device A (the upper figure in **Fig. 3**), which is microfabricated on a 2×2 mm chip. The current capacity of device A is designed to be approximately the same as that of device B. The electrode widths and electrode-to-electrode spacings are as shown in the figure.

Figure 4 shows the top view of device A. A 2×2 mm chip is divided into four unit-transistors for the purpose of increasing active area or decreasing on-resistance compared with a single unit-transistor of the same size. Device B has the same fundamental design as device A, but its chip size is 3×3 mm and 6 unit-transistors are on a chip. Both device A and device B are designed to have the same current capacity of 2.5 A on a chip.

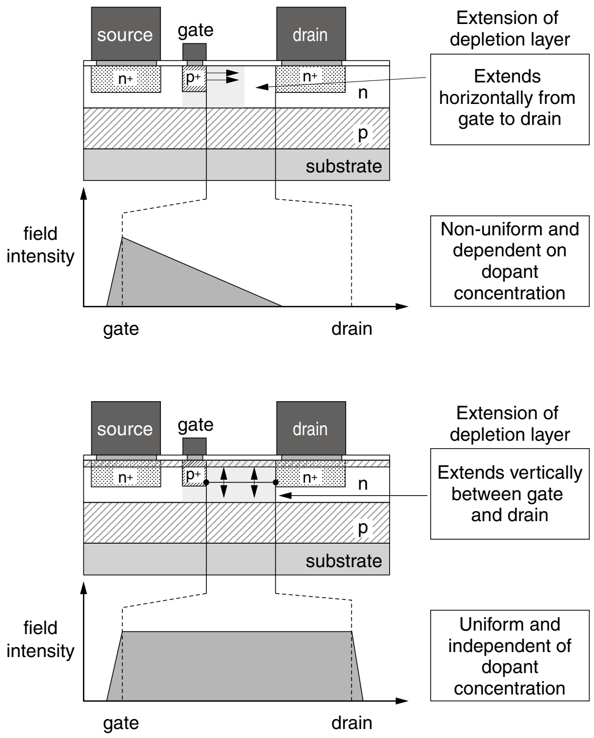

Fig. 2. Features of RESURF-JFET

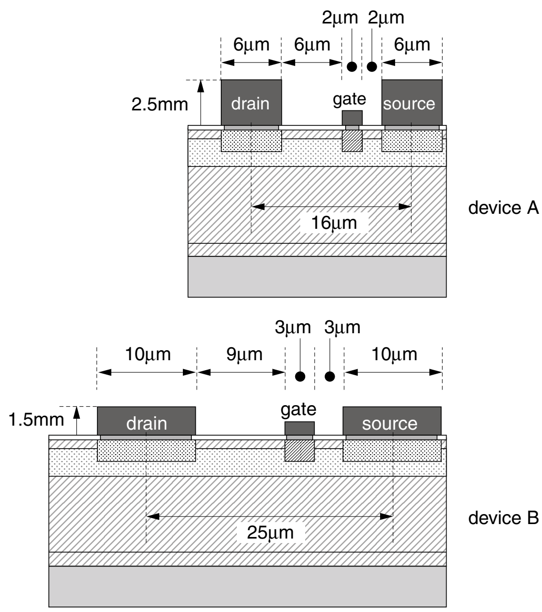

Fig. 3. Cross-sectional views of devices A and B

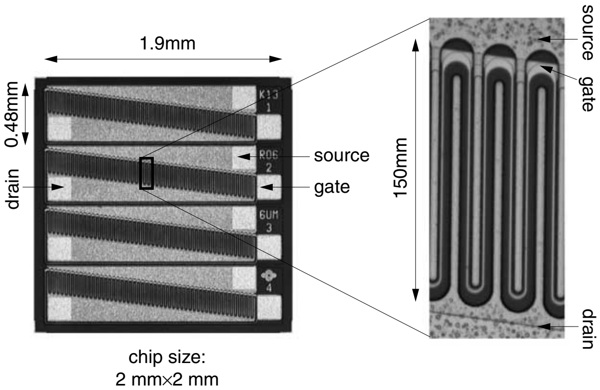

Fig. 4. Top view of device (A)

2-3 On-wafer fabrication process

Figure 5 shows the on-wafer fabrication process of RESURF-JFET. The process is similar to that reported in the previous paper (3), except the use of microfabrication technology.

(a) Epitaxial growth

The four epitaxial layers of 4H-SiC are grown on a 400-μm-thick and 8 degrees off-axis (0001) substrate using chemical vapor deposition (CVD).

(b) Device isolation

Each substrate area on which a unit-transistor will be formed is isolated from others by trenches made by a kind of dry etching process called reactive ion etching (RIE).

(c) Ion implantation

To form the regions of the source, drain and gate electrodes, n-type and p-type area-selective doping is carried out by ion implantation. First, after a metal mask layer is formed over the entire substrate surface and windows are opened on the mask by RIE at the source and drain regions, phosphorus (P) ions are implanted through these windows. Next, once again the residual mask is removed, a mask layer is formed and windows are opened at the gate regions, and then aluminum (Al) ions are implanted to the gate regions. To prevent damage to the SiC crystal structure during ion implantation, the wafer is heated to about 500˚C during the implantation process.

(d) Annealing for dopant activation

To electrically activate the implanted dopants and repair crystal damages caused by implantation, the wafer is annealed at about 1700˚C in argon ambient. When a SiC surface is exposed to ambient and annealed and heated to such a high temperature, the surface roughens. To suppress surface roughening, a cap layer is formed by spin-coating photoresist layer on SiC and heating it to be graphitized.

(e) Formation of oxide film

A SiO_2 oxide layer of 0.1 μm thickness is formed on the surface by heat treatment at 1300˚C in dry oxygen ambient for 60 minutes. This oxide film is used for surface protection.

(f) Formation of ohmic electrodes

Ohmic contacts are formed as the source, drain and gate electrodes. First, windows are opened on the field oxide layer and a nickel (Ni) layer of 0.1 μm thickness is deposited on the surface of SiC. Next, to obtain ohmic contacts, the wafer is heated at about 1,000˚C in argon ambient so that Ni is alloyed with SiC.

(g) Formation of wiring and pad

A transistor having a large current capacity is obtained by electrically connecting more than one small transistor in parallel with one another. A gate wire having a thickness of 0.1 μm is formed by vacuum evaporating Al. A SiO2 insulation layer of 0.3 μm thickness is formed between the gate wire and the source wire by plasma CVD. The drain wire and the source wire both have a thickness of 2.5 μm. A Ti layer is formed under each Al wire to enhance interfacial adherence .The surface of the device is covered with a 2 μm-thick SiO2 passivation layer using plasma CVD. Windows are formed on the passivation layer at the pad region.

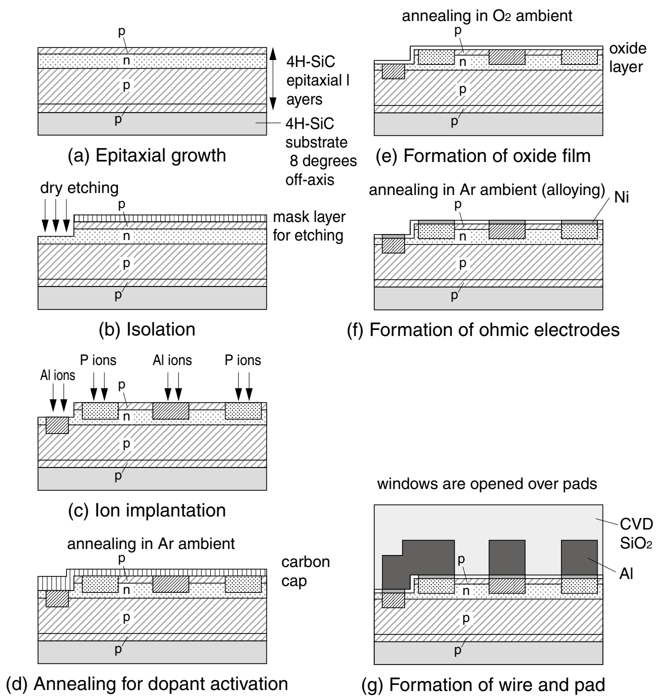

Fig. 5. Fabrication process of RESURF-JFET

2-4 Packaging

After the completion of the on-wafer process, screening was carried out by electrical characteristics measurement. The selected chips are mounted on a TO-220 package (**Fig. 6**), whose base is made of Cu-W that exhibits high thermal conductivity.

(a) Dicing

The fabricated wafer is cut into unit chips using a dicer

(b) Mounting

A chip is mounted on a TO-220 package and adhered by solventless silver paste.

(c) Bonding

On the chip, four unit-transistors are connected in parallel with each other using gold (Au) wires.

(d) Burying

To provide insulation between Au wires, silicone gel is filled until the wires are buried completely.

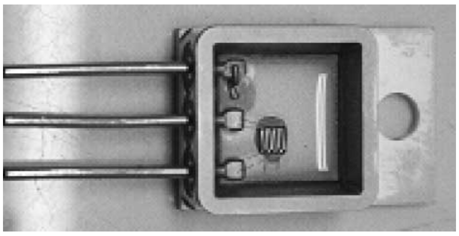

Fig. 6. Appearance of TO-220 package with chip

3. Characteristics and applications of RESURF-JFET

Static, capacitance and switching characteristics were measured for the packaged transistor samples.

3-1 Static characteristics

The static characteristics of device A at room temperature was measured using a curve tracer. **Figure 7** shows the drain current (I_D) versus drain voltage (V_{DS}) curves for different values of gate voltage (V_{GS}).

The drain current was successfully controlled by the gate voltage. In the region of low drain voltage, the drain current increased linearly and showed a tendency to saturate as the drain voltage increased, showing typical FET characteristics. Because the drain current was 2.5 A at V_{GS} = 2 V and V_{DS} = 2.15 V, the on-resistance was 0.86 O. The active area of the chip was 6.0×10^{-3} cm^2. Therefore, the specific on-resistance (the product of on-resistance and device's active area) was 5.2 mOcm^2. The linear increase continued up to the drain current of 5V, which is twice the value of the rated current 2.5 A. In the saturation region the drain current was 7.5 A at V_{GS} = 2 V, V_{DS} = 10 V.

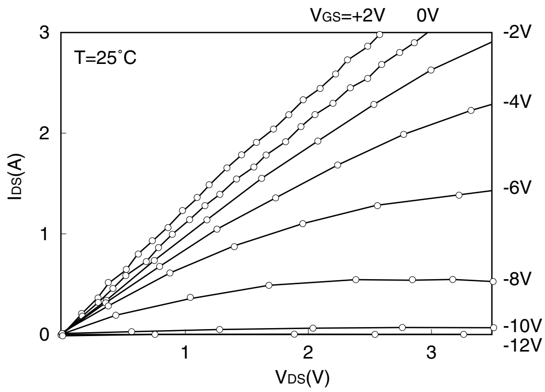

Fig. 7. Drain current (ID) versus drain voltage (V_{DS}) for different values of gate voltage (V_{GS})

Figure 8 shows the dependence of saturated drain current and on-resistance on chip size for devices A and B. Compared with device B, device A exhibited not only a larger current capacity and a lower specific on-resistance but also a smaller chip size.

Figure 9 shows the blocking characteristics of device A. The gate cut-off voltage was -15 V. In the off state, no breakdown of the device was observed at drain voltages smaller than 400 V. The breakdown voltage of device A was estimated to be approximately 600 V according to the breakdown test result of the test device for device A.

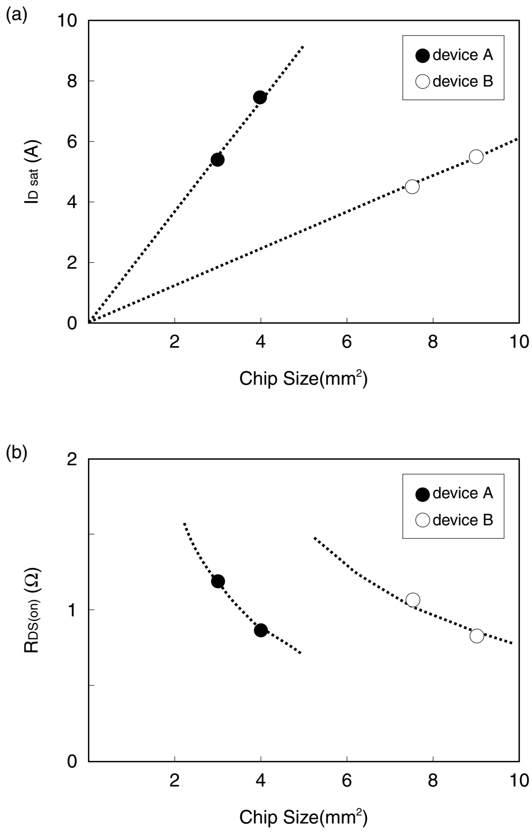

Fig. 8. Chip-size dependence of a) saturated drain current and b) on-resistance for devices A and B

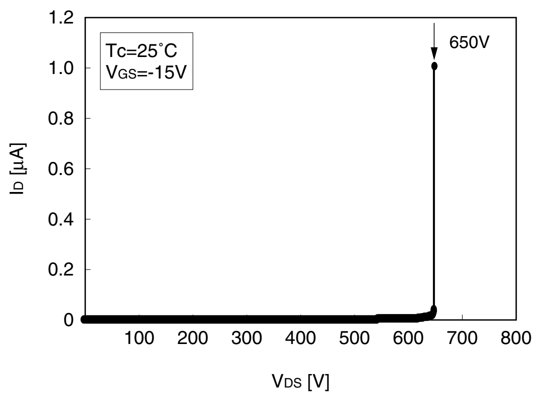

Fig. 9. Blocking characteristics of test device for device A

The on-resistance of device A was one-tenth of that of an 800-V-class RESURF-JFET, which was reported 50 mΩcm^2 in the previous paper [3]. The typical on-resistance of a Si MOSFET whose blocking voltage is 400 V and rating current is 2.5 A is about 2.5 Ω. The on-resistance of device A was a half that of the Si MOSFET.

3-2 Capacitance characteristics

Figure 10 shows the typical capacitance characteristics measured using an impedance analyzer.

The gate-source capacitance and drain-gate capacitance at V_{DS} = 30 V were 60 pF and 9 pF, respectively. The capacitance of device A is reduced to 50% that of device B. Compared with a typical 400 V/2.5 A Si-MOSFET, device A exhibited a smaller gate-source capacitance.

Capacitance characteristics are indicators of switching characteristics, so the decrease of capacitance indicates the improvement of fast switching characteristics.

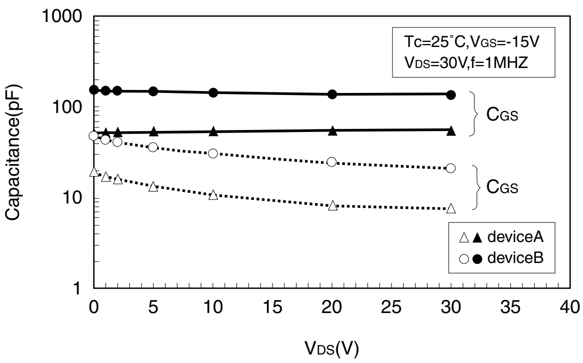

Fig. 10. Drain current versus capacitance characteristics for devices A and B

3-3 Switching characteristics

Figure 11 shows an evaluation circuit for measuring resistance load switching characteristics. The load voltage (V_{DD}) was 60 V and the resistance was 22 Ω. The drain current was 2.5 A.

As the driving signal, a pulse was applied to the gate electrode of the device from a pulse generator. The amplitude of the pulse voltage was 20 V and the bias was -18 V, that is, the pulse voltage for the on and off states were 2 V and -18 V, respectively. The pulse width was 1 µm. The driving circuit gate resistance (R_G) was 2.5 Ω. The measurement was carried out at 25˚C. **Figure 12** shows the typical resistance load switching characteristics waveforms of V_{DS}, I_D, and V_{GS} for device A.

In the turn-on operation, the turn-on delay time ($t_{d(on)}$) was 3 ns and the turn-on rising time (t_r) was 5 ns, making the total turn-on time (t_{on}) 8 ns. In the turn-off operation, the turn-off delay time ($t_{d(off)}$) was 4 ns and the turn-off falling time (t_f) was 6 ns, making the total turn-off time 10 ns. Since the switching time of a typical 400 V/2.5 A Si MOSFET is about 20 ns, 4H-SiC RESURF-JFET can switch two or three times faster than Si MOSFET.

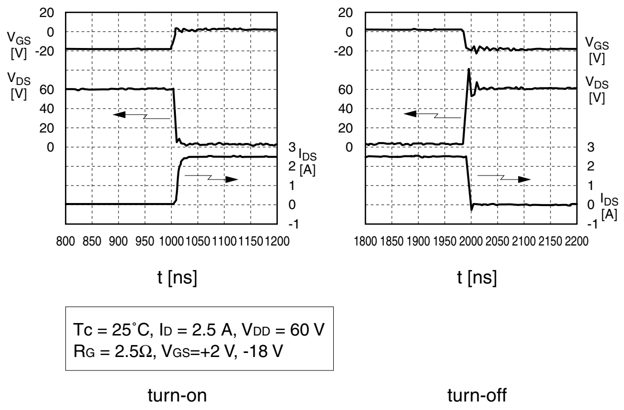

Fig. 12. Resistance load switching characteristics

Figure 13 shows an evaluation circuit for detecting inductive load switching characteristics, and **Fig. 14** shows the typical inductive load switching characteristics waveforms of device A. The supply voltage (V_{DD}) was 100 V. The drain current was set to 2.5 A by controlling the pulse width of the driving pulse. The driving circuit gate resistance (R_G) was 5 Ω. Other conditions were the same as those in the case of resistance load switching.

Figure 15 shows the typical switching time versus gate resistance characteristics during inductive load switching.

The total turn-off time of device A was 9 ns at R_G = 5

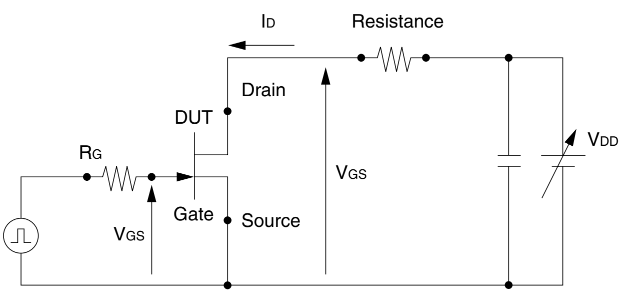

Fig. 11. Evaluation circuit for measuring resistance load switching characteristics

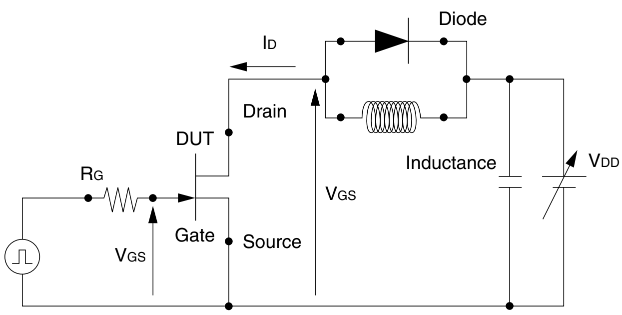

Fig. 13. Evaluation circuit for measuring inductive load switching characteristics

O. The turn-off delay time ($t_{d(off)}$) was 5 ns and the turn-off falling time (t_f) was 4 ns. Fast switching was confirmed during inductive load switching just as during resistance load switching. Compared with that of device B, the turn-off time of device A was more than 20% shorter as is shown in **Fig.16**.

As mentioned above, miniaturized device A has a smaller capacitance and faster switching time than device B. It is expected that switching time will be made faster in the future by developing more miniaturized devices.

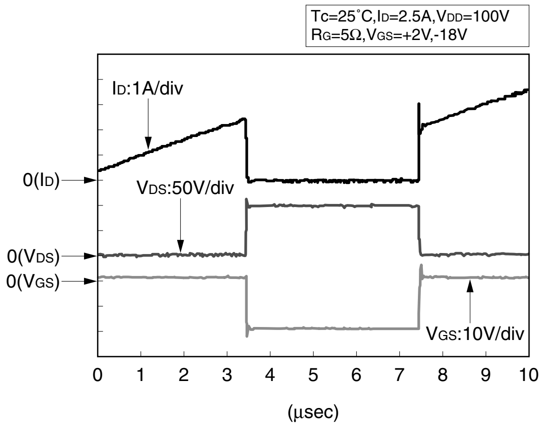

Fig. 14. Inductive load switching characteristics

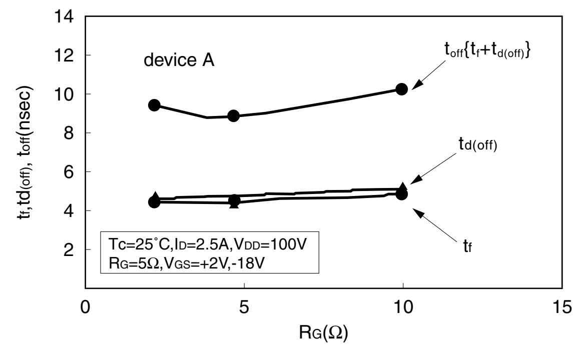

Fig. 15. Switching time versus gate resistance

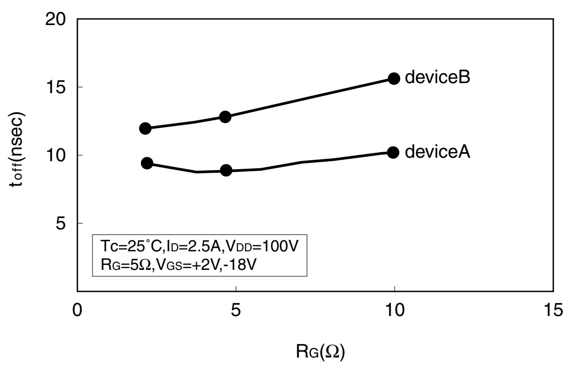

Fig. 16. Turn-off time vs gate voltage

4. Prospects

The fabricated SiC RESURF-JFET has advanced characteristics of high breakdown voltage (about 600 V), low on-resistance (5.2 mOcm^2) and fast switching time (less than 10 ns). These characteristic values exceed the physical limits of Si and are many times superior to those of a Si MOSFET that has the same breakdown voltage and current handling capability. Therefore, although the SiC lateral RESURF-JFET is inferior to vertical devices in the area of high current applications, the authors considered that in the area of low to medium current applications it can be used as a high-voltage, low-loss, fast-switching device that contributes to the advancement of power electronics equipment.

The typical low- or medium-current switching power supplies in which Si-MOSFET or IGBT are used are DC/DC converters and DC/AC converters. The technology trends in this application area are towards smaller equipment size and higher efficiency. One way of downsizing switching power supplies is the use of high-frequency switching power devices. However, the power loss increases as the frequency at which a power device carries out the switching operation increases. This means that in high-frequency operations it is necessary to decrease not only on-resistance loss but also switching loss. Therefore, both low on-resistance and fast switching capability are required for power devices.

Furthermore, a protection circuit is typically added for preventing the breakdown of a power device due to the surge voltage generated in the high frequency operation, but the protection circuit generates power loss. Therefore, a high breakdown voltage needs to be guaranteed for a power device to endure the surge voltage. By applying a power device that has a high breakdown voltage and fast switching ability, protection circuit can be deleted and equipment size can be reduced.

These requirements can be fulfilled by applying the SiC RESURF-JFET having a proprietary device structure, and it is expected that a power electronics system can be made smaller and more efficient than when using a Si device.

Functions that were not added previously due to limited space can be added and the value added to the system can be heightened.

As mentioned above, the SiC RESURF-JFET is a device expected to be applied to the switching power supplies for low or medium current handling.

5. Conclusion

The authors have developed a SiC RESURF-JFET that exceeds the physical limits of Si power devices. The fabricated sample transistor showed the characteristics exceeding the physical limits of Si devices: Low on-resistance, fast switching capability and advanced properties due to miniaturization. Because the fabricated device can accomplish large-current switching at a fast-switching speed at several hundred V, the device is expected to be applied to switching power supplies.

Sumitomo Electric continues to work toward realizing lower on-resistances and faster switching speeds by developing the technologies for microfabricating the transistor patterns and improving the design and fabrication processes, as well as developing a switching power supply that carries a RESURF-JFET.

6. Acknowledgement

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