History of Ion Implanter and Its Future Perspective

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Nissin Ion Equipment Co., Ltd. has been engaged in the manufacturing and sales business of medium current ion implanters for manufacturing semiconductor devices since its establishment. The EXCEED series has been widely acknowledged by the device manufacturers for its quality in the basic machine concepts and for its continued supplies of the leading-edge models that meet ever-changing customer requirements. This paper outlines improvements in the system performance and the key technology of the EXCEED series, such as magnetic energy filter, radio frequency (rf) plasma flood gun, precise implant angle control and high throughput end station. The paper also looks toward the technology for future ion implanters.

Keywords: medium current implanter, energy filter, implant angle control, end station

1. Introduction

In 1999, Nissin Ion Equipment Co., Ltd., which was previously engaged in business under the name of Ion Equipment Department of Nissin Electric Co., Ltd., has become independent as a 100%-owned subsidiary of Nissin Electric Co., Ltd. At that time, EXCEED2000, an ion implanter that Nissin Electric had developed in 1994 with the new technology of energy contamination-free for the first time in the world, started gaining recognition for its value. That was also the time when EXCEED2000A was consecutively brought to the market with its greatly improved productivity.

As a result of the booming economy and growth in the IT sector in Asia since 1999, we have successfully managed to expand our business not only in Japan but also in the East Asia. Ever since then, the EXCEED series has been recognized as one of the most leading-edge ion implanters for its continuously upgraded performance in response to the sophistication of process needs.

In this paper, the technical history of ion implanters is described on the basis of technological enhancement in the EXCEED series and its expected future development is also presented.

2. Semiconductor Manufacturing Processes and Our Ion Implantation Equipment

The basic structure of a semiconductor IC MOSFET (Metal Oxide Silicon Field Effect Transistor)[1] is schematically shown in **Fig. 1**. Dimensions of each element in a transistor are determined by a scaling law of the gate length (Lgate). **Figure 2** shows types of transistors, which are classified according to the application as DRAM, Flash Memory, LSTP (Low Stand-by Power)[2], LOP (Low Operational Power)[3], MPU/ASIC (Micro-Processor/Application Specific Integrated Circuit)[4]. Each Lgate and Line-Pitch is in a proportional relation. The half-length of DRAM Line-Pitch, called node, represents the reference length for the transistor and it has been continuously

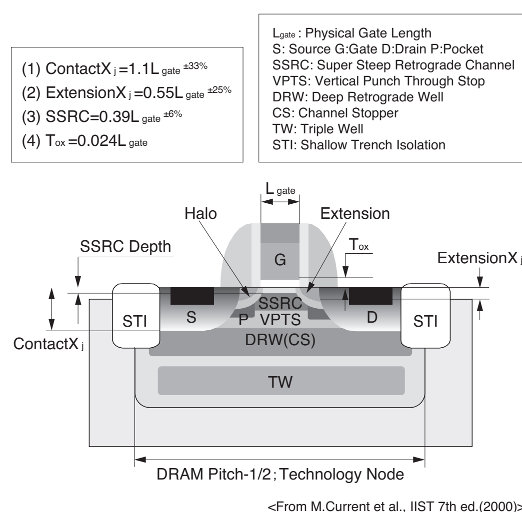


Fig. 1. Transistor Structure and Scaling Law for Implantation Process

reduced by 30% in every three years. This is well known as “Moore’s scaling law." High integration and shrinkage for the IC have been advanced according to this scaling law with the device density doubled in three years. The miniaturization has remarkably improved IC performance and, at the same time, reduced cost per information unit (bit). This way the IC market has grown continuously. So the scaling is the driving force of the semiconductor business. Although some people concern about the possibility of the end of the scaling law in near future, the history shows that such a concern has been overcome again and again in the past by the development of new technologies. Through the development of ion implantation equipment, our company has played a certain role in developing these technologies and will do so in the future.

Typical IC transistors are P-type MOSFET and N-type MOSFET, in which a positive hole dominant layer (P-layer) and an electron dominant layer (N-layer) contact each other and make a junction. The P-layer is made by implanting an electrically positive dopant, such as boron ion, into silicon, while the N-layer is made by implanting an electri-

ITRS 2007 Prospect for 1/2 Pitch & Gate Length

Year of production	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022
DRAM 1/2 pitch (nm)	100	90	80	70	65	57	50	45	40	36	32	28	25	22	20	18	16	14	13	11
Flash Poly Si 1/2 pitch (nm)					54	45	40	36	32	28	25	23	20	18	16	14	13	11	10	9
MPU/ASIC Metal 1(M1) 1/2 pitch (nm)					68	59	52	45	40	36	32	28	25	22	20	18	16	14	13	11
LSTP Physical gate length (nm)	76	65	53	45	45	37	32	28	25	23	20	18	16	14	13	11	10	9	8	7
LOP Physical gate length (nm)	65	53	45	37	32	28	25	23	20	18	16	14	13	11	10	9	8	7	6.3	5.6
MPU physical gate length (nm)	45	37	32	28	25	23	20	18	16	14	13	11	10	9	8	7	6.3	5.6	5.0	4.5

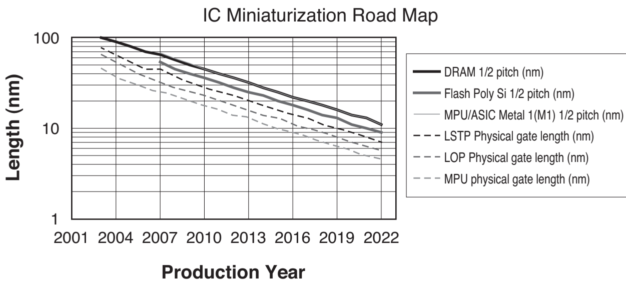


Fig. 2. IC Miniaturization Roadmap

cally negative dopant, such as phosphorus or arsenic ions, into silicon. A P-type MOSFET consists of P+N+P silicon junctions, and an N-type MOSFET consists N+P+N junctions. The P-type MOSFET and N-type MOSFET are combined into a CMOSFET (Complimentary MOSFET)[5], which is a basic unit of the IC logic circuit. A typical manufacturing process for a single level Vt (Threshold Voltage)[6] CMOSFET is shown in **Table 1**. This table illustrates how many ion implantation processes are necessary. In this example, the ion implantation processes involve 11steps, but the number of implantation steps for the most-advanced multiple Vt level CMOS, such as three or four Vt level CMOS, increases to more than 30 steps. In semiconductor manufacturing plants, the following four types of ion implantation equipment are used according to the amount of the energy and dose required for each implantation process: a high current implanter (HC), medium current implanter (MC), high energy implanter (HE) and ultra-high dose doping implanter (UHD).

Figure 3 shows the range of the energy and dose that the four types of ion implanters cover. Nissin Ion Equipment has been dealing with the medium current implanter. By concentrating its resources on the EXCEED

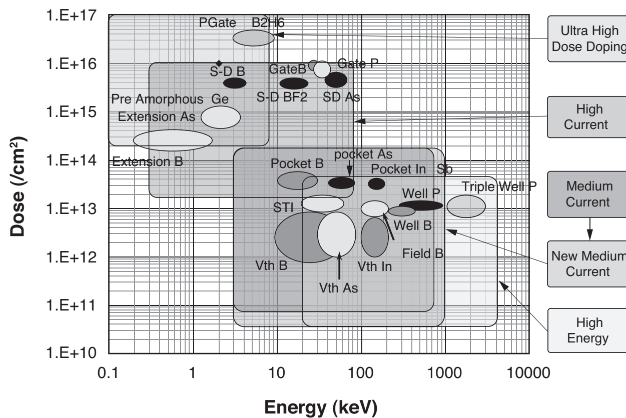


Fig. 3. Ion Implantation Process and Ion Implanter Classification

Table 1. Ion Implantation Process Step

No.	Process for double well CMOS		Current CMOSFET(1999 ~)	
(Well formation)				
1	High resistivity n-type Si wafer		10Ω - cm	
(Field Oxide Layer formation)				
2	Field SiO2 layer	Thermal Oxidation	SiO2 under layer for LOCOS	
3	Si3N4 layer	CVD		
4	Resist Coating			
5	Photo Etching	Mask 1	To implant below p-field oxide layer	
6	Dry Etching (Si3N4)			
7	Resist Removal		P channel resist stripping	
8	Resist Coating			
9	Photo Etching	Mask 2	To implant below n-field oxide layer	
10	Dry Etching (Si3N4)			
11	Field Oxidation	Steam Oxidation		
(Gate formation)				
12	Si3N4 · SiO2 Underlayer removal		for LOCOS formation	
13	Dumas or HCl Oxidation		Gate Layer formation	
14	Resist Coating			
15	Photo Etching	Mask 3	To implant n-channel	
16	B Implantation	300 ~ 1000keV, 1E13	N-channel well formation & channel stopper	HE
17	B or In Implantation	40 ~ 100keV, 1E12	N-channel punch-through stopper	M
18	B Implantation	20 ~ 50keV, 1E12	N-channel Vth control	M
19	Resist stripping			
20	Resist Coating			
21	Photo Etching	Mask 4	To implant p-channel	
19	P Implantation	600 ~ 3000keV, 1E13	P-channel well formation & channel stopper	HE
22	P or Sb Implantation	80 ~ 150keV, 1E12	N-channel punch-through stopper	M
23	P Implantation	40 ~ 100keV, 1E12	N-channel Vth control	M
24	Resist stripping			
(p-channel Source Drain formation)				
25	Poli-Si Film formation	SiH4 ThermalCVD	for gate electrode formation	
26	Resist Coating			
27	Photo Etching	Mask 5	for p-channel gate electrode formation	
28	Dry Etching (Poli-Si)	CF3 gas	P-gate formation	
29	B Implantation	1 ~ 10keV, 2E14	P-channel extension & p-gate doping	LE
30	SiO2 Film formation	CVD		
31	Side Wall formation	RIE		
32	Post Treat.			
33	B or BF2 Implantaion	10 ~ 50keV, 2E15	P-channel source drain implant	H
34	Resist stripping			
(n-channel Source Drain Formation)				
35	Resist Coating			
36	Photo Etching	Mask 6	for n-channel gate electrode formation	
37	Dry Etching (Poli-Si)	CF3 gas		
38	P Implantaion	5 ~ 30keV, 2E14	N-channel extension & n-gate doping	LE
39	SiO2 Film formation	CVD		
40	Side Wall formation	RIE		
41	Post Treat.			
42	As Implantaion	20 ~ 50keV, 5E15	N-channel source drain implant + gate implant	H
43	RTA	1000°C	S/D activation	
44	Side Wall process with HF	HF		
45	Co + TiN Film formation			
46	Saliside RTA #1 step			
47	TiN Removal	Sulfate Cleaning		
48	Saliside RTA #2 step			
(Electrode formation)				
49	PSG-CVD Film formation	P Glass Film	Interlayer dielectric formation	
50	Reflow	1000°C	Surface planarization for wiring	
51	Resist Coating			
52	Photo Etching	Mask 7	Source drain contact formation	
53	Dry Etching (PSG)			
54	As Implant for Contact	30 ~ 50keV, 5E15/cm²	Reduction of contact resistance	H
55	Si added Al Spputering	Si, 1 ~ 3%	To avoid alloy pit	
56	Resist Coating			
57	Photo Etching	Mask 8	Source drain wiring	
58	Dry Etching (Al)	BCl3 Gas		
59	H2 Anneal	400 ~ 600°C	To improve Si-SiO2 interface, To stabilize of S/D contact	

Photo Etching Process 8 cycles HE ; 2 step M ; 4 step H ; 5 step (LE ; 2 step)

series, our company has expanded the global presence in the medium current industry and held about 30% share since 2004. In 2007, by integrating an innovative technology of cluster ion sources and the field-proven technology of EXCEED series, a ultra-low energy implanter “CLARIS” was released to the implanter market.

3. Nissin Ion Implanter and Its Key Technology Evolution

3-1 Overview of the evolution

Improvements in the systems and performance of EXCEED series ion implanters are summarized in **Fig. 4**. In 1994, EXCEED2000 medium current ion implanter was developed, featuring the world’s first energy filtering function. EXCEED2000A was released in 1998 with dramatically improved reliability of the end station. In 2000 EXCEED2300H, compatible for 300 mm wafers, in 2001 EXCEED2300V, capable of indium implantation, in 2003 EXCEED2300AH, embodying greatly improved mechanical throughput (maximum capacity), in 2005 an authentic 300 mm medium current implanter EXCEED3000AH, realizing remarkably increased beam current and mechanical throughput, and in 2007 EXEED9600A with an expanded energy range were released to the market one after another. Furthermore, in 2010, EXCEED-Evo series was launched as a highly productive tool for next-generation process.

Thus, from the EXCEED2000 to EXCEED-Evo2, upgraded new products have been successively developed and released to the market in about every two years, in keeping with the process evolution over 6 generations from 210 nm node to 45 nm node. The density advancement in the 6-generation evolution is 32 fold. The wafer size has also shifted from 200 mm in the past to 300 mm at present, and 450 mm wafer is said to be put into production in the next five years, which promises productivity improvement of four times.

Productivity improvement with enlarged wafer and miniaturized IC cannot be achieved without ion implanters of further improved performance. As shown in **Fig. 4**, for productivity improvement it is absolutely necessary to raise

	Year of Production	'94	'95	'96	'97	'98	'99	'00	'01	'02	'03	'04	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16
	Tech. Node DRAM 1/2 Pitch (nm)	240	210	190	165	150	140	135	130	115	100	90	80	70	65	57	50	**45**	**40**	**36**	**32**	**28**	**25**	**22**
	EXCEED2000/2000A/2000AH		2000			EXCEED2000A / 2000AH																		
	EXCEED2300H/2300AH							2300H			AH													
	EXCEED2300V/2300V<G1>/<G2>								2300V		2300AV			2300AV<G2>										
	EXCEED3000AH<G1>/<G2>/Evolution												G1	3000AH<G2>				EXCEED3000AH-Evo						
	EXCEED9600A/Evolution														EXCEED9600A			EXCEED9600A-Evo						
EXCEED Productivity	Wafer Size		200mmφ					300mmφ													**450mmφ**			
	Mechanical Throughput		200wf/H					220wf/H			300wf/H		360	450wf/H										
	Beam Current: B+		250 uA @ 10keV					250 uA @ 10keV					1200 uA @ 10keV											
	Beam Current: As+		400 uA @ 20keV					500 uA @ 20keV					500 uA @ 20keV											
	Beam Current: B++		40 puA @ 500keV					30 puA							250 puA									
	Beam Current: P+++		15 puA @ 600keV					15 puA							85 puA									
	Min. Energy		10 keV					5 keV					3 keV											
	Max. Energy		400 keV					750 keV							960 keV									
	Ion Source Type		Bernas					Advanced Bernas (BEAR)							IHC type (IHC-R2)									
	Set Up Time		6 min					4.5 min			3.5 min		3.0 min					**2.5min**						
	Maintenance Time (I/S Life Time)		200H					400H							700H									
EXCEED Preciseness	Indium							Indium-																
	Energy Contamination		Final Energy Magnet -																					
	Particle Contamination							Conductive-Peek Wafer Holder -																
	Metal Contamination										Metal Free Cover -													
	Uniformity		1D-2L			2D-2L		2D-3L Faraday System -																
	Parallelism / Beam Divergence														X-Y monitor			**Vertical Lens Feedback Control System**						
	Tilt/Twist Angle Accuracy																	**Wafer Angle Feedback Control System**						
	Charge Compensation					Filament PFG			RF-PFG									**N-PFG**						
	Patterning Implantation (PI System)															PI System								

Fig. 4. Performance Evolution of EXCEED Implanters

the mechanical throughput and beam current, to extend the ion source life, and to shorten the setup time. For further miniaturization of the IC, it is important to control ion implantation precisely. The control is realized by a variety of technologies, such as high precision repeatable control for dose uniformity and implant angle, elimination of device damage caused by the charge-up during implantation, filter-out of various types of contamination, generation of new ion beams, and patterning implantation (PI)[(7)] to compensate the variation of transistor characteristics across the wafer. These key technologies need to be integrated in a harmonious way. The following sections describe how the integrations have been achieved.

3-2 EXCEED2000A

Figure 5 shows a schematic of EXCEED2000A equipped with the single platen type end-station. It consists of an ion source, analyzer magnet, acceleration tube, energy filter magnet (FEM), beam sweep magnet (BSM), collimator magnet (COL), and end station. All EXCEED products adopt this configuration. EXCEED2000, which is the first type of the EXCEED series, had a drawback of the poor operational reliability of the end station, although it featured a novel dual-platen structure and embodied a position-fixed implantation throughout wafer scanning. EXCEED2000A achieved a dramatically improved productivity and effective throughput, by employing a single platen structure which significantly ameliorated operational reliability and maintainability.

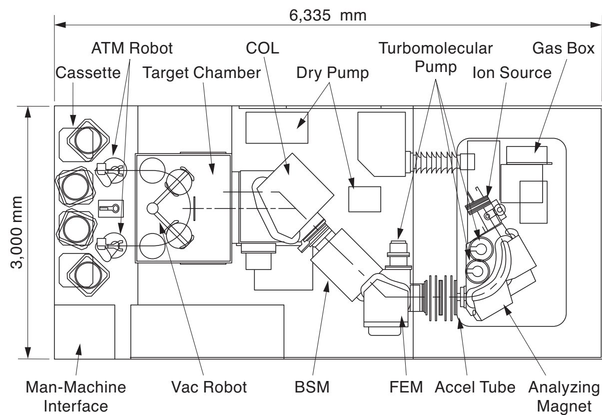


Fig. 5. Schematic Layout of the EXCEED2000A

FEM is one of the functional elements characterizing the EXCEED series, that is, it completely removes energy contamination components contained in the beam after acceleration. Energy contamination is likely to vary in its density and changes the dopant density depth profile in an uncontrolled way. Thus a fine energy contamination filter like FEM is indispensable to suppress the Vt variation of transistors. **Figure 6** shows the structure of beam line in the vicinity of FEM. Energy contamination components contained in the beam after acceleration or deceleration are removed completely with a slit (aperture) provided at the beam entrance of BSM. Energy contamination compo-

nents are generated due to the dissociation and/or the ionization reaction by collision of ion beam particles with residual gas particles in the vicinity of the accelerating tube. Once the beam is implanted with the energy contamination component, the implanted dose and depth can deviate from the aimed value. The collision reaction that causes energy contamination is a serious problem when molecular ions or multiply charged ions are used as a dopant. Energy contamination is problematic because, although bare wafers for test implantation do not cause major energy contamination due to little out-gassing during implantation, it becomes so much worse for the production of resist-coated wafers due to the increase of residual gas pressure by outgassing during implantation. Energy contamination is also subject to fluctuations depending on the operating condition of the evacuation system. The use of FEM completely removes the energy contamination components, allowing molecular ions or multiply charged ions to be used in the production process. At present, it becomes standard for medium current implanters to implement some energy filtering components in the beam line. Of those energy filtering components, kinetic momentum separation systems like FEM have the greatest capability of energy contamination removal in terms of the system configuration.

In EXCEED series, the ion beam is scanned by a biased scanning magnetic field of the BSM excited by AC current with DC biased, and then is made parallel by the COL's magnetic field. The magnetic beam scanning, an exclusive technology to Nissin Ion, effectively reduces the loss of beam because the blow-up of the beam caused by the space charge effects is suppressed. The reason for using the biasing magnetic field is to eliminate beam paths passing in the field of zero regions so that a possible spatially localized anomalous variation of space charge is excluded.

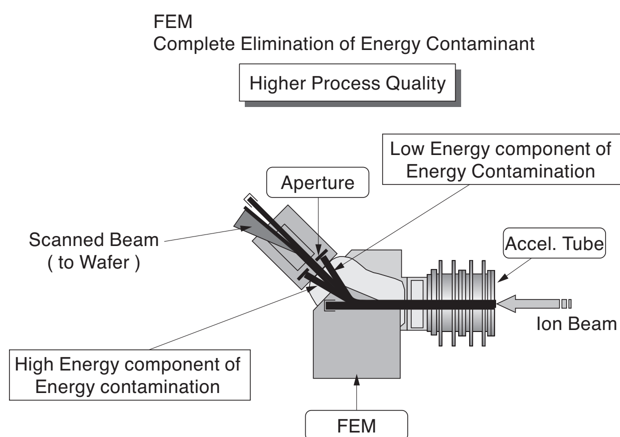


Fig. 6. Energy Filtering Magnet (FEM)

Figure 7 shows the configuration of the implantation system to control the uniformity of implanted ions across the wafer plane. The control technology for implantation serves as the foundation of the high precision and reliable implantation of the EXCEED series. In the system, the scanned beam current profile is measured at each position on the front Faraday array and back Faraday array respectively located in front of and at the back of the wafer position so that the dose distribution along the scanning direction at the wafer can be precisely estimated with these two current profiles. To make the dose distribution uniform, the system iteratively synthesizes waveform of the BSM coil current until the uniformity of dose distribution sits within a reference range. In addition to monitoring and controlling the dose distribution at the wafer position, this system can measure beam parallelism or angle distribution of the scanned beam along the scanning direction. Nissin Ion Equipment's NH20-SP, a main implanter before the EXCEED series, had the built-in function of monitoring the beam parallelism for the first time in the world. For the EXCEED series, the monitoring function of beam parallelism was improved in terms of reliability, accuracy and speed. Further improvements on this system are presented in the next section.

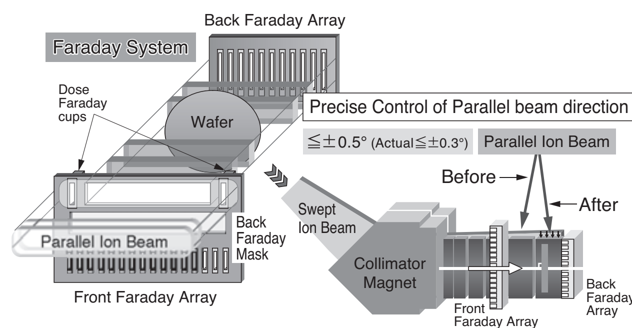


Fig. 7. Multiple Faraday System for Monitoring/Tuning Dose Uniformity and Beam Parallelism

3-3 ECEED2300H/AH/V, EXCEED3000AH

In 1996, almost immediately after the development of EXCEED2000A for 200 mm wafers, EXCEED2300H was developed for processing 300 mm wafers. It was soon qualified as a 300 mm wafer production tool by SELETE (Semiconductor Leading Edge Technologies, Inc.), a consortium consisting of 10 semiconductor manufacturers in Japan, and released to the market in 1998. EXCEED2300H has a hardware configuration of a scaled-up end station and ground-potential portion of the EXCEED2000A beam line, while several architectures, such as the control software/hardware for automated beam tuning, implant control and wafer handling control, were maintained to facilitate the development.

Marketability of a production tool for 300 mm wafers highly depends on its mechanical throughput in terms of technological differentiation. EXCCE2300AH increased the number of wafer exchange positions in a vacuum from one to two, and provided a buffer station for wafer transportation in the atmospheric side, thereby achieved a throughput increased by 40% compared with that of the EXCEED2300H.

For the miniaturization of the transistor structure, in place of boron or phosphorous ions, heavier ions like

indium or antimony ions have come to be used since the beginning of 2000 in order to make the implantation depth or the junction depth shallower. For this purpose, a new beam line with a high magnetic field was developed to handle heavy ions. At the same time, a new ion source system equipped with a high temperature vaporizer was also developed. Employing these new components, EXCEED2300V was launched to the market in 2001.

Figure 8 is a schematic diagram of EXCEED3000AH, which was released in 2005 for 300 mm wafer processing. This equipment markedly increased amount of the beam current compared with EXCEED2300V by spreading the beam passage through the beam line. For the end station, the conventional solid two-armed wafer handling robot system in the vacuum was replaced with the independently movable two-armed robot. In addition, the single-armed robot in the atmospheric side was replaced by the dual-armed robot with three mechanical joints, and the wafer centering by rotating wafer on the wafer aligner was eliminated. These changes improved the mechanical scanning speed by 60%. The boron beam current at 10 keV was also increased by 2.5 times. In total the system increased its throughput by 50%. In **Fig. 9**, the traditional end station equipped in EXCEED2300AH and the throughput – enhanced end station in EXCEED3000AH are illustrated with the difference emphasized.

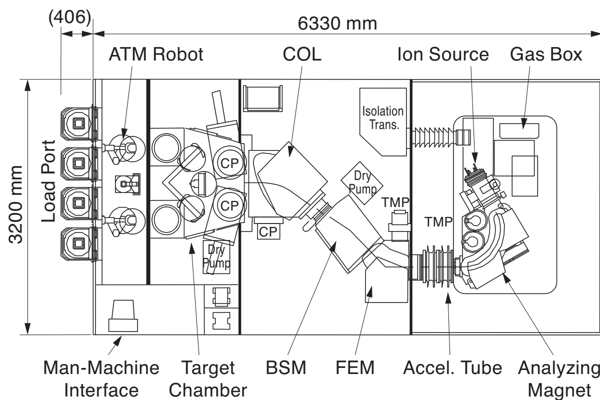


Fig. 8. Schematic Layout of the EXCEED3000AH

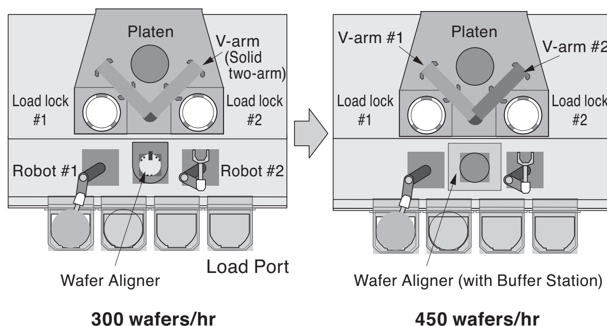


Fig. 9. Throughput Upgrade in End station

In today's ion implantation process, spatial uniformity of the beam implantation angle and its reproducibility are important factors for the IC device miniaturization. For example, in the Halo implantation, the beam angle accuracy is a determining factor of the Vt variation and has to be maintained in high precision. **Figure 10** shows a sophisticated beam parallelism/azimuth measuring method (referred to XY monitor) employed in EXCEED3000AH. The traditional measuring method for horizontal beam parallelism/azimuth angle distribution and beam divergence distribution is depicted on the left side. The right side of the figure shows that by adding a servo motor drive to the Faraday and slit in the vertical direction, the new measuring system is enabled to measure the vertical azimuth angle and beam divergence distribution. These parameters related to the beam angle can be adjusted to a predetermined value by the ion source beam extraction electrode and the beam optical components in the beam line system. With this function, the system can obtain information about the scanned beam shape at any locations in the beam scanning direction. This means that the measuring system can be used as a useful tool for real-time monitoring of the process of judging the dose distribution, and also for checking the uniform angle distribution at the implantation. On the other hand, accuracy and reproducibility for tilt and twist angles of wafers on the platen during implantation are also very important elements for guaranteeing angle accuracy. The overview of the system for controlling and monitoring twist and tilt angles is shown in **Fig. 11**. Employing a CCD camera above the platen to detect the wafer position, this system performs a feedback control at an accuracy of ±0.1 degrees. As the gate length shown in **Fig. 1** becomes short according to the progress of miniaturization, the threshold voltage Vt apparently tends to vary depending on the position on the surface of the wafer because the sensitivity of Vt value against the variation of the gate length becomes much higher. Therefore, even a small change in the amount of gate etching between the central position and the peripheral position can induce a big change in the Vt value. To compensate the Vt change according to the radial position on the wafer, it is proposed

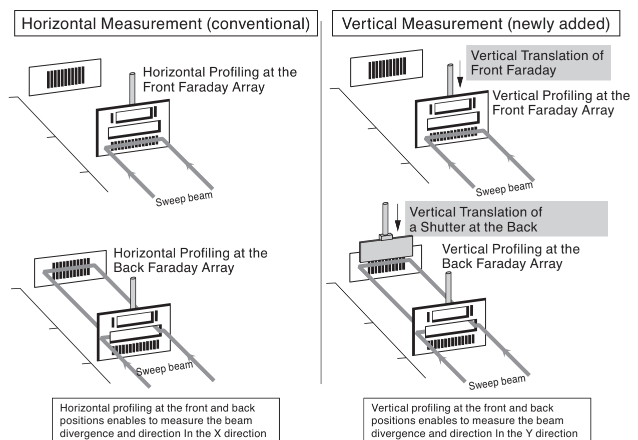


Fig. 10. Two Dimensional Measuring/Tuning Mechanism of Scanned Beam Angles (X-Y Monitor)

to ramp the implantation dose from the central position to the peripheral position on the wafer. That is, instead of uniform dose distribution on the entire wafer surface, a well-controlled non-uniform implantation (concentric distribution) is to be used for this specific purpose of compensating non-uniformity characteristics of the former process. Implantation control in EXCEED3000AH addresses these needs, taking advantage of a step rotation of the wafer and a program control of the wafer scanning speed.

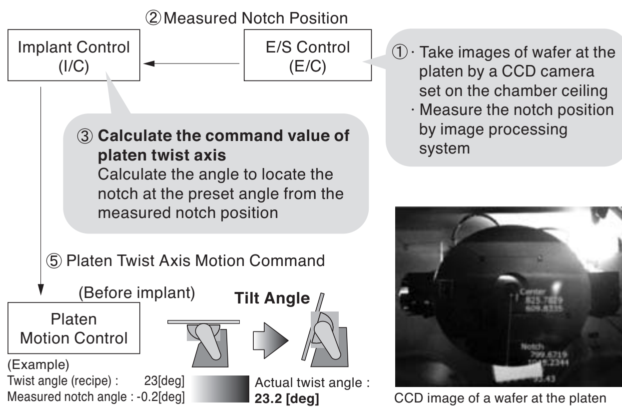


Fig. 11. Monitoring System for Tilt and Twist Angles of Wafer

3-4 EXCEED9600A

Figure 12 is a schematic diagram of EXCEED9600A, which has increased the maximum implant energy for singly charged ion from 250 keV to 320 keV, for doubly charged ions to 640 keV, for triply charged ion to 960 keV. As shown in **Fig. 3**, the energy range of medium current machines is increasing. Due to device miniaturization, the majority of existing high-energy processes have lowered the implant energy in the range that the medium current implanter can handle. Thus, the High energy MeV implanter would only treat the expensive high-energy processes and sub-MeV energy processes will be executed by the medium current implanter, thereby production efficiency of the entire implantation process will be improved. In EXCEED9600, the voltage applied to the acceleration tube has been raised from 210 kV to 270 keV by modifying the acceleration tube and acceleration power supply of the EXCEED3000AH. Considering clean room environments, a molded isolation transformer, which was optionally installed in the EXCCED3000AH, is applied as a standard component. Appropriate insulating space is also preserved between the voltage-shielding cabinet and the high-voltage terminal to minimize the footprint of EXCEED9600A.

To generate the multiply-charged high-current ion beam with long life, EXCEED9600A employs an indirectly heated cathode-active reflection (IHC-R[9]) ion source, which was newly developed by significantly improving the hot cathode structure of the exiting Bernas source and the Bernas-type electron active reflection (BEAR[8]) source. The BEAR ion source and the IHC-R ion source are shown schematically in **Fig. 13**. In a BEAR ion source, as its name suggests, electrons are reflected on the plasma production region when variable voltage is applied to the reflector electrode. Efficiency in forming ion beams is improved by increasing the plasma density at the vicinity of the ion extraction slit, reducing the load to the filament and extending its service life. On the other hand, in an IHC-R ion source, a plate cathode positions between the plasma and the filament so that the filament is not exposed directly to the plasma. The cathode is heated by the energetic electrons emitted from the filament, and emits thermionic electrons to produce the plasma. The reflector voltage of the IHC-R ion source has a similar configuration of that of the BEAR ion source. Modification of the insulation material used in the cathode area has raised the operating temperature limit, improving the source's heat and dirt resistance. Production efficiency of highly charged ions, as well as singly charged ions, has been improved, leading to the satisfactory long-life operation for highly-charged ions. **Figure 13** shows the maximum beam currents and the cathode life for the two types of ion source.

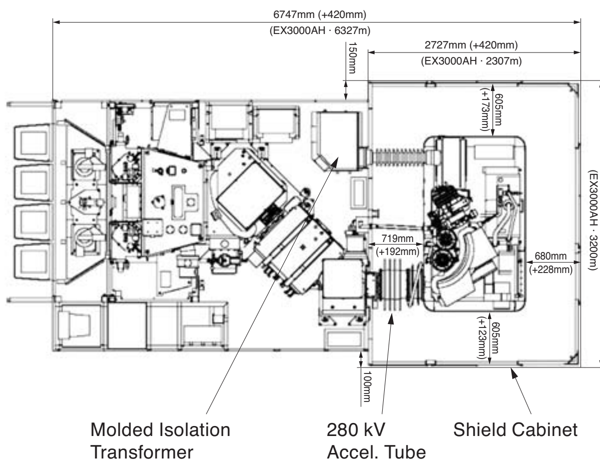
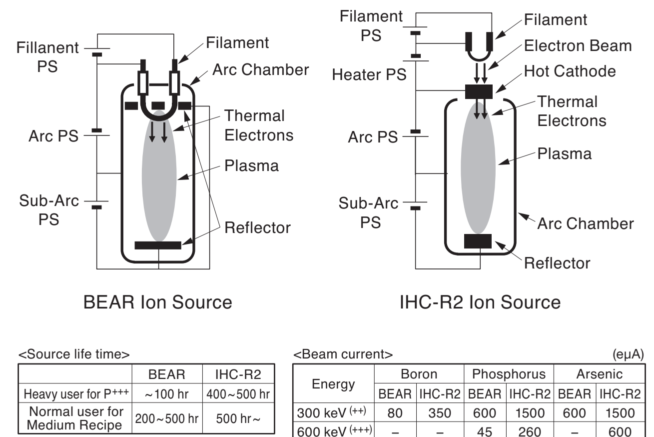


Fig. 12. Schematic Layout of the EXCEED9600A



<Source life time>

	BEAR	IHC-R2
Heavy user for P^{+++}	~100 hr	400~500 hr
Normal user for Medium Recipe	200~500 hr	500 hr~

<Beam current> (eμA)

Energy	Boron		Phosphorus		Arsenic	
	BEAR	IHC-R2	BEAR	IHC-R2	BEAR	IHC-R2
300 keV $^{(++)}$	80	350	600	1500	600	1500
600 keV $^{(+++)}$	–	–	45	260	–	600

Fig. 13. Scematics of Two Types of Ion Sources

3-5 EXCEED3000AH-Evo/9600A-Evo

EXCEED3000AH-Evo and EXCEED9600AH-Evo were released in 2010 with 27% upgraded productivity as a result of the comprehensive systematic improvements of EXCEED3000A and 9600A for their wafer handling, maximum ion beam currents, down time of the entire system, etc. On the wafer transfer system, the wafer transfer robot program has been optimized and the operating speed of the implantation unit has been increased by 20%.

The beam current at low energy below 20 keV has been increased 20% by adding an electrostatic lens (V-lens). The downtime has been reduced by refining the entire control algorithm for the automated beam setup step and implantation step, minimizing the frequency of error-stop occurrence, and enhancing the error recovering function. In addition, the system has shortened the time to pump out the released gas during implantation by adding cryopumps to enhance its evacuation capacity for the target chamber, which aims to reduce overall processing time. Some of these technologies can be retrofitted to the old EXCEED products.

3-6 Other key technologies for IC miniaturization

As the beam current increases, coupled with IC device miniaturization, fatal damage may be caused to ICs due to the electrical charge-up. To solve the charge-up problem, two types of charge compensation systems, shown in **Fig. 14**, have been developed. For implantation to wafers up to 200 mm, EXCEED2000AH employs a filament-type plasma flood gun (PFG), and for 300 mm wafers, EXCEED2300H adopts an RF-type PFG. Both systems supply plasma electrons to the beam and eventually to the wafer in order to compensate the ion beam positively charged on the wafer. In order to prevent the plasma electrons from giving an excess negative charge to the device on the wafer, the electron energy must be less than 3 eV, corresponding to the oxide breakdown voltage of 1 nm or less thin gate oxide. The RF-type PFG, shown in **Fig. 14**, can supply such low energy electrons by magnetic filtering. As the PFG has no tungsten filament, tungsten contamination and other filament-life problems can be prevented in principle. For this reason, it has become an indispensable component of ion implanters used for the latest device fabrication.

With the progress of device miniaturization, it has become increasingly important to prevent contamination of metal and other particles. EXCEED3000AH, EXCEED9600A and Evo series have thoroughly equipped with graphite shields and the like having qualities of high purity and less-particle generation in order to cover the surface of the area facing the beam and to block metal and other particle contamination from the upstream beam line (SAM).

4. Future Ion Implantation Technology and Our Course of Action

Figure 15 shows the roadmap for the next generation transistor structures, which is extracted from the semiconductor roadmap released by International SEMATECH: ITRS2009 (International Roadmap for Semiconductor 2009). It is expected that the conventional poly-silicon gate transistors with SiO_2 gate oxide are to be replaced with metal gate transistors with High-k gate dielectric, followed by further shift to the next generation transistors, such as FD-SOI (Fully Depleted-Silicon on Insulator) [11] and Multi-Gate transistors by 2013. However, regarding the devices that need extremely high reliability such as CCD/CMOS sensors and DRAM/Flash Memory, it has not yet been verified whether they are to be mass produced with such next generation transistor structures without any particular problems.

Since highly precise implantation is required for manufacturing miniaturized devices with reliable performance, continued evolution of EXCEED3000 Evo and EXCEED9600 Evo should be conducted. Meanwhile, the low-energy high-dose implantation process for future transistors can be done by CLARIS<G1>, which was released in 2008 as a dedicated tool for Boron implantation and upgraded to CLARIS<G2> in 2009 by adding carbon implantation functions. CLARIS<G3> with phosphorus and arsenic implantation functions is scheduled to be released in 2011. As the CLARIS series covers almost all energy ranges for the high current implanter, all the implant processes, except for high energy MeV implantation, can be carried out using EXCEED and CLARIS series.

	Filament Type PFG	RF Type PFG
Electron Energy	6 eV	3 eV
Electron Current Density	10 µA / cm²	20 µA / cm²
Life Time of PFG	> 500 hr	> 1000 hr

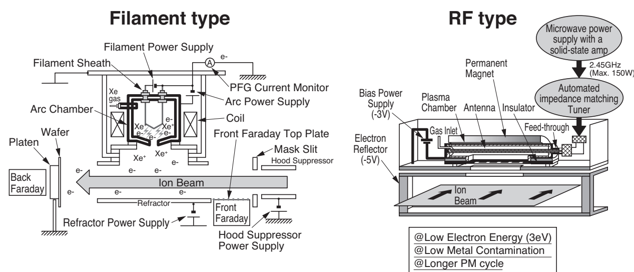


Fig. 14. Charging Reduction Systems: Filament Type and RF Type

Production Year		04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
Technology Node (nm) DRAM 1/2 Pitch		90 nm			65 nm			45 nm			32 nm			22 nm			16 nm	
Technology Node (nm) Flash Poly Si 1/2 Pitch		–			54 nm			36 nm			25 nm			18 nm			13 nm	
Poly-Si Gate (Classical MOS)																		
Metal High-k Gate	Bulk-MOS																	
	FD-SOI																	
	Multi Gate																	
450mm Wafer Production																		

Next Generation Device ⇒ High-k Metal Gate, FD-SOI, Multi Gate

Fig. 15. ITRS 2009 Roadmap

In **Fig. 15**, a prediction of wafer size expansion is also shown. The leading semiconductor business companies, such as Intel Corporation, Samsung Electronics Co., Ltd., and Taiwan Semiconductor Manufacturing Company, Ltd., are considering manufacturing a 450 mm wafer by 2015. In response to this market need, we intend to develop a new implanter compatible with 450 mm wafers.

Finally, ion implantation technology's application fields other than semiconductor IC fabrication are outlined. SiC devices have attracted much attention recently because of their potential as next-generation devices used in low-power consuming appliance or electric vehicles. Since SiC devices are resistant to high temperature, they are expected to markedly improve the inverter's efficiency and to be used as power device transistors including in-vehicle transistors. It used to be difficult and costly to make large SIC substrates over 4 inches, and the market remained small. However, methods of making high-quality SiC substrates larger than 6 inches have been recently developed, increasing the possibility of raising the production yield by the use of ion implantation technology. For SiC devices, we have released ImpHeat, an ion implanter capable of implanting Al ions of high beam current to substrates at high temperature. This product will contribute to the SiC device market by improving productivity and reducing costs in SiC device production.

Applications of ion implantation to the fields of MEMS and Solar cell mass production can be feasible, if implanters that can provide great performance are released at low costs.

Twenty years ago, Nissin Ion Equipment introduced an ion implanter for manufacturing low temperature poly silicon thin film transistors (LTPS-TFTs) to the field of manufacturing high precision displays. Since then we have delivered large-scale implanters for processing substrates of generation 4.5, followed by implanters for generation 5 and 5.5 substrates, in response to growing needs in the high definition smart phone market.

5. Conclusion

The ion implanter has to be continuously upgraded in its performance in order to meet the needs for high precision and productivity associated with progressing IC device miniaturization. We have been working on the development of new model implanters and released such products in every two years by improving our original technologies, such as magnetic filtering of energy contamination, high precise monitoring of implantation angle and high throughput end station. We intend to provide advanced implanters that meet the needs of ever-evolving technology for the semiconductor industry.

* EXCEED, CLARIS and IMPHEAT are registered trademarks of Nissin Ion Equipment Co., Ltd.

Technical Term

*1 MOSFET (metal oxide silicon field effect transistor) : A field-effect transistor most commonly used in large-scale integration.

*2 LSTP (low standby power) : A type of MOSFET of low standby power. Used primarily in cellular phones.

*3 LOP (low operational power) : A type of MOSFET of low operating power. Used mainly in personal computers.

*4 MPU/ASIC (micro-processor/application specific integrated circuit) : A semiconductor chip for basic computing/A large-scale integration designed and manufactured for specific applications. High speed operation and high power consumption.

*5 CMOSFET (complimentary MOSFET) : A transistor system that has both P-type and N-type MOSFETs on the same circuit. High speed operation and low power consumption.

*6 Vt (threshold voltage, voltage threshold): A threshold voltage of digital IC on/off control.

*7 PI (patterning implantation) : A method of controlling the distribution of implantation in injection to the wafer plane.

*8 BEAR (Bernas-type electron active reflection) : An ion source with a filament load reduced by the improvement of Ion generation efficiency. A variable voltage is applied to a Barnas ion source plasma generator to activate electron reflection.

*9 IHC-R (indirectly heated cathode-active reflection) : An ion source that has a cathode between the plasma and the filament to prevent direct exposure to the plasma. The cathode generates plasma electrons using thermal electrons from the filament. Enables long service life and an increased amount of multivalent ion beams.

*10 ITRS2009 (International Roadmap for Semiconductor 2009 Edition) : A roadmap for semiconductors published in 2009 by International SEMATECH. ITRS2010 follows ITRS2009 in the basics.

*11 FD-SOI (fully depleted-silicon on insulator) : A fully depleted transistor of ultra-low power consumption.

*12 LTPS-TFT (low temperature poly silicon thin film transistor) : A low-temperature poly-silicon thin film transistor. Used for switching pixels of a high-definition display.

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