Development of E-band Transmitter Chipset Using Wafer Level Chip Size Package Technology

Atsushi YONAMINE*, Miki KUBOTA, Osamu BABA, Koji TSUKASHIMA, Tsuneo TOKUMITSU and Yuichi HASEGAWA

We have developed a transmitter chipset using a new tripler, up-converter, and power amplifier, and arranged the chipset in a transmitter. Monolithic microwave integrated circuits (MMICs) of these devices are designed using our wafer level chip size package (WLCSP) technology, and reflow-soldered on a 16 mm x 12 mm printed circuit board (PCB). The WLCSP technology enables the development of highly integrated package-free flip-chip MMICs suitable for surface mounting, and is therefore expected to reduce production costs significantly. To achieve high performance at the E-band frequency, 1) the amplifier is designed with a dual or triple high electron mobility transistor (HEMT) topology, with the power amplifier designed with a variable gain scheme, 2) The tripler effectively cancels the second harmonic of input signals that otherwise leak into the E-band frequency, and 3) the up-converter uses a balanced resistive mixer and a pair of 90° broadside couplers. The transmitter that incorporates these new devices exhibits a conversion gain of 22 dB and saturated output power level of 20 dBm at 81 - 86 GHz.

Keywords: 3D-MMIC, WLCSP, E-band, transmitter

1. Introduction

E-band wireless communication systems are expected to be widely used for short-distance broadband services and networking due to their high transmission rates. These E-band wireless communication systems use wide frequency bands of 71-76 GHz and 81-86 GHz, and therefore, the development of cost-saving devices in these frequency bands is essential.

This paper describes new monolithic microwave integrated circuits (MMICs) that we have developed for E-band communication systems. These MMICs are used in a tripler, up-converter (U/C), and power amplifier (PA) through the application of three-dimensional monolithic microwave integrated circuit (3-D MMIC) technology and wafer level chip size package (WLCSP) technology[1],[2]. The 3-D MMIC technology enables high integration and the WLCSP technology eliminates the need for both wiring and packaging, thus contributing to production cost savings. We evaluated the performance of these new MMICs by mounting them on a printed circuit board (PCB) as a form of an E-band transmitter chipset.

2. Component of the E-band Transmitter Chipset

Figure 1 shows an E-band transmitter chipset that consists of the new tripler, U/C, and three PAs. The mounting area of the transmitter chipset is 16 mm x 12 mm as indicated by the dashed line in the figure.

Figure 2 shows the cross sectional view of the WLCSP structure. The MMIC surface is covered with a common ground metal layer partially being removed for pads. A number of small-circle ground pad attachments are periodically formed on the MMIC surface. The WLCSP structure can be mounted on the PCB through the solder-reflow process, and the solder balls arrayed on a die provide a good interconnection even at millimeter-wave frequencies. The WLCSP technology enables the development of highly integrated circuit devices and package-free flip-chip MMICs suitable for surface mounting[3]-[8].

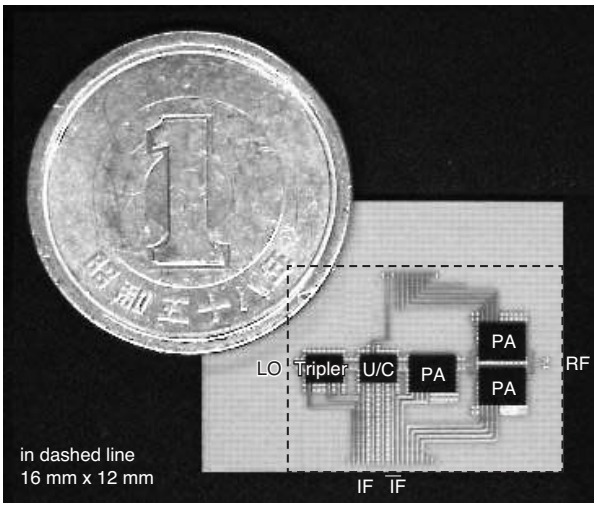

Fig. 1. E-band transmitter chipset

Figure 3 shows a transmitter block diagram and MMIC components. Local oscillator (LO) signals are converted into x3LO signals (from 65 GHz to 92 GHz) by the tripler. The x3LO signals are mixed with intermediate frequency (IF) signals by the U/C and output as RF signals. The RF signals are then amplified by the 2-stage PAs. At the final stage of the parallel PAs, the signals are provided with sufficient output power for E-band communication systems.

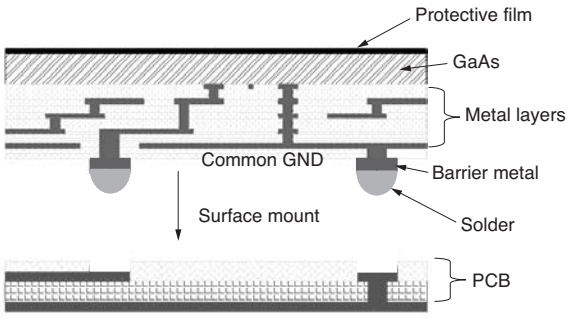

Fig. 2. Cross sectional view of WLCSP

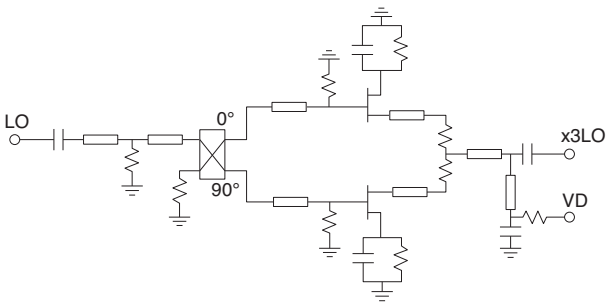

Fig. 5. Circuit schematic of the tripler

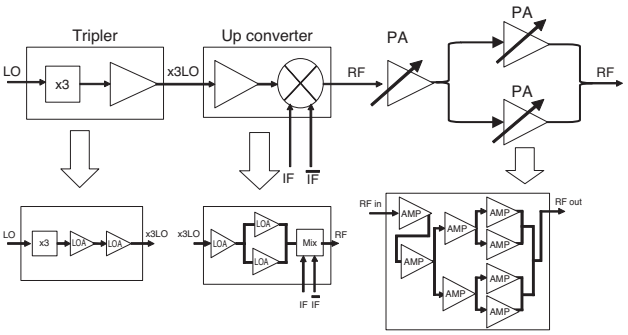

Fig. 3. Block diagram of the transmitter and MMIC configuration

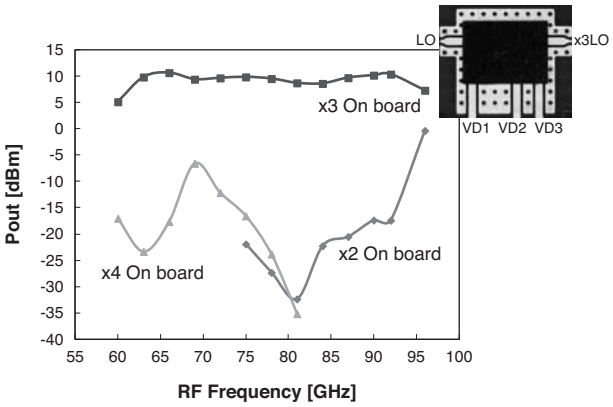

Fig. 6. Output performance of the tripler

3. Tripler and Up-Converter

Figure 4 shows the MMIC of the tripler and its block diagram. The size of this MMIC is 2.3 mm x 1.7 mm.

The tripler MMIC is composed of a tripler circuit and two LO amplifiers. The circuit schematic of the tripler is shown in **Fig. 5**, in which the rectangle with a cross indicates a 90° coupler, and 0 and 90° indicates signal phases at the coupler ports. Spurious signals are suppressed by the tripler circuit and the gain characteristics of the LO amplifier. The tripler provides x3LO signals without using filters. The LO amplifier uses the reuse-type triple-HEMT[*1] for high gain.

The output performance of the on-board tripler is shown in **Fig. 6**. The x3LO signal power level is more than 7 dBm at 65-92 GHz and spurious signal power level is lower than the x3LO signal power level by 15 dB.

Figure 7 shows the MMIC of the U/C and its block diagram. The size of this MMIC is 2.3 mm x 1.7 mm.

The U/C MMIC is composed of x3LO amplifiers and a balanced mixer. The x3LO amplifier uses Dual-HEMT[*1]. The gate width of the HEMT is 40 μm x 4 to achieve broadband gain characteristics. x3LO amplifiers at the second stage are combined together with Wilkinson combiners to saturate the conversion gain of the mixer.

The circuit schematic of a balanced mixer is shown in **Fig. 8**, in which the circle with a cross indicates a resistive mixer.

The balanced mixer is composed of a pair of resistive mixers and 90-degree couplers. The x3LO signal leakage is canceled, and the RF signals are combined at the RF port.

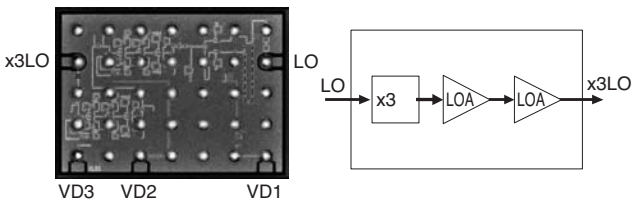

Fig. 4. The MMIC of the tripler and its block diagram (MMIC size: 2.3 mm x 1.7 mm)

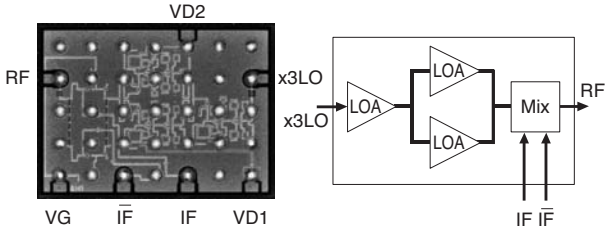

Fig. 7. The MMIC of the U/C and its block diagram (MMIC size: 2.3 mm x 1.7 mm)

As shown in **Fig. 9**, the conversion gain of the on-board U/C is nearly -15 dB. The IF input power level is -7 dBm. The IF frequencies are 6-18 GHz.

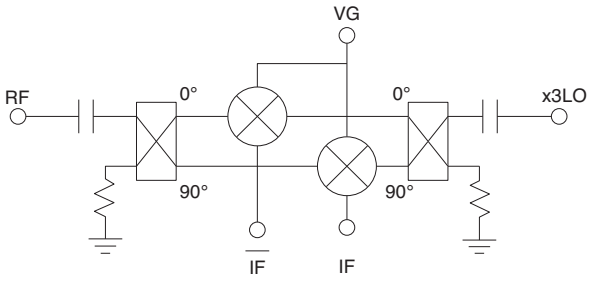

Fig. 8. Circuit schematic of the balanced mixer

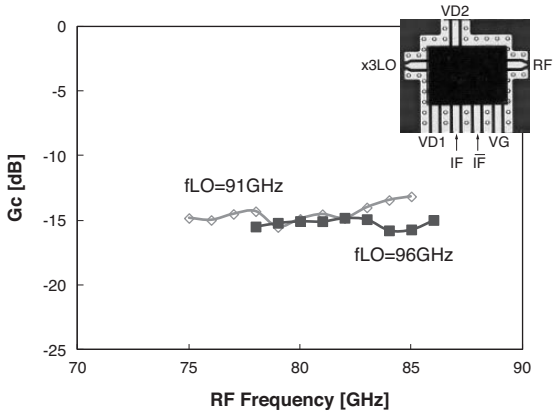

Fig. 9. Conversion gain of the U/C

4. Power Amplifier

Figure 10 shows the MMIC of the PA and its block diagram. The size of the MMIC is 2.9 mm x 2.3 mm.

The PA is designed to have four stages (series amplifiers) to obtain a high gain of 20 dB. The PA is also designed to have four parallel unit amplifiers in its final stages to obtain high output power level at 18 dBm. The circuit schematic of the unit amplifier is shown in **Fig. 11**. The

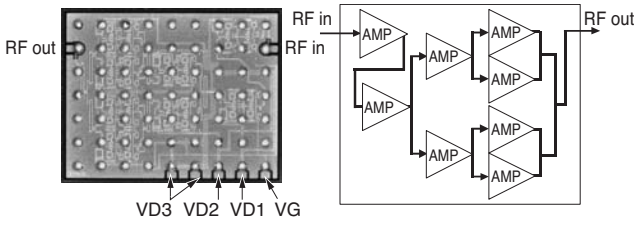

Fig. 10. The MMIC of the PA and its block diagram (MMIC size: 2.9 mm x 2.3 mm)

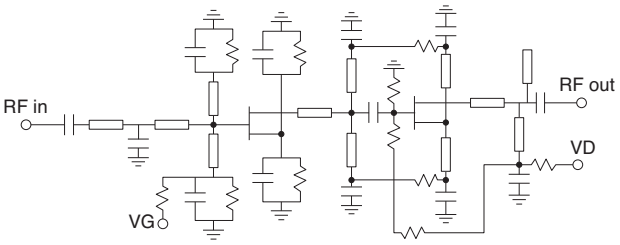

Fig. 11. Circuit schematic of the unit amplifier

gate width of the unit amplifier is 50 μm x 6. The gain variation is performed with the gate voltage of the first HEMT. The gate voltage of the second HEMT is fixed with the resistor circuitry.

The frequency characteristic of the on-board PA is shown in **Fig. 12**. The output power of the PA is shown in **Fig. 13**. The PA gains 20 dB at 81-86 GHz. The saturated power levels are 18.7 dBm at 81 GHz and 19.1 dBm at 86 GHz. The total power consumption is 2.4 W.

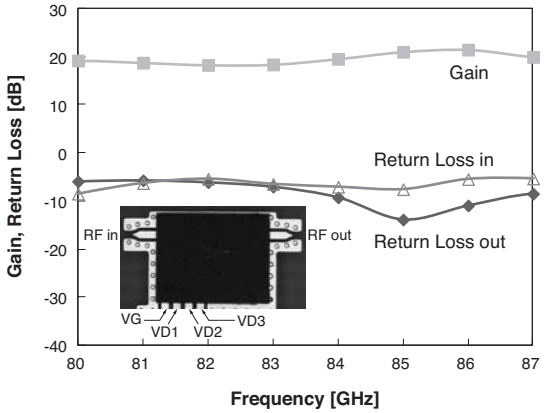

Fig. 12. Frequency characteristic of the PA

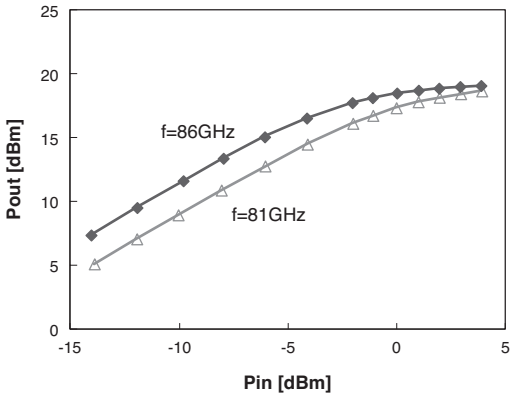

Fig. 13. Output power of the PA

5. E-band Transmitter

A set of the MMICs developed for E-band transmitters were mounted on a PCB through the solder-reflow process to assess the transmission gain and output power performance.

The conversion gain of the transmitter is shown in **Fig. 14**. The output power of the transmitter is shown in **Fig. 15**. The conversion gain is 22 dB, and the saturated power levels are 20.1 dBm at 81 GHz and 19.7 dBm at 86 GHz. The total power consumption is 7.8 W.

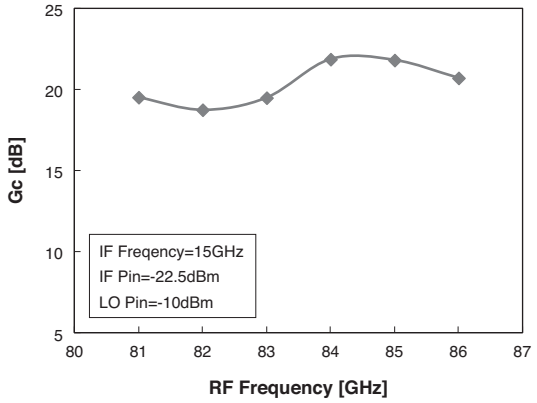

Fig. 14. Conversion gain of the transmitter

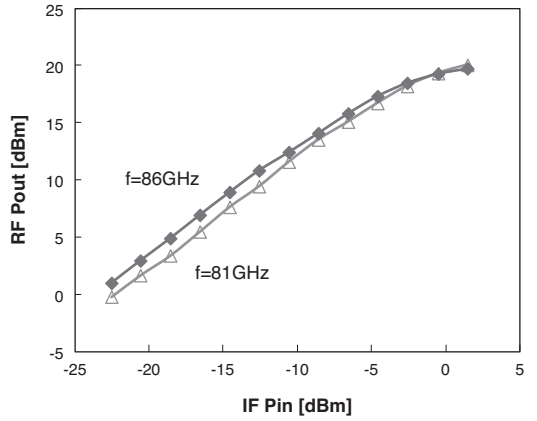

Fig. 15. Output power of the transmitter

6. Conclusion

This paper presented the design summary and measurement performance of the E-band transmitter chipset. As compared with conventional E-band products, the E-band transmitter chipset using WLCSP technology is expected to offer high productivity at a low price. The transmitter chipset consists of the new tripler, U/C, and three PAs assembled on the PCB by solder-reflow process. The mounting area of the transmitter chipset is 16 mm x 12 mm. The transmitter achieves a conversion gain of 22 dB and saturated power levels of 20.1 dBm at 81 GHz and 19.7 dBm at 86 GHz. The total power consumption is 7.8 W. This is the first time for Sumitomo Electric Industries, Ltd. and Sumitomo Electric Device Innovations, Inc. to achieve this high performance from the E-band transmitter chipset. We will make our best effort to achieve further high output power performance.

Technical Term

*1 Dual-HEMT, Triple-HEMT: Transistor structures in the current reuse topology. A continuous DC-current path is formed through two or three transistors such as HEMTs. These are often used to enhance gain.

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