Low Capacitance Gate Process for E-Band GaN HEMTs

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Gallium Nitride (GaN) is superior in breakdown voltage and RF performance and is suitable for high electron mobility transistors (HEMTs). Since wireless communication using millimeter-wave E-band (70–80 GHz) features wide bandwidth and large capacity, this system has been expected to function as backhaul communication. Therefore, we decided to develop E-band GaN HEMTs. The HEMT we aimed to develop required exclusive high frequency compared to that of current products that use mainly micrometer-waves (up to 16 GHz). So we had to remarkably improve RF performance. We chose InAlN as a barrier of GaN HEMTs for high transconductance and developed low capacitance gate process, a key technology of RF performance improvement. To reduce gate capacitance (C_{gs}), Y-shaped gate process with short gate length of 100 nm was developed. With this process, we have obtained extremely low C_{gs} of 0.58 pF/mm and the current gain cutoff frequency of 110 GHz and realized high RF performance E-band GaN HEMTs.

1. Introduction

Gallium Nitride (GaN) is suitable for high electron mobility transistors*1 (HEMTs), because the breakdown voltage and electron velocity of GaN are higher than those of Gallium Arsenide (GaAs) and Silicon (Si). Now, RF GaN HEMTs are necessary for wireless communication infrastructure.

GaN HEMTs have been developed with the rapid growth of cellphone and smartphone markets. We released the world's first GaN HEMTs for the amplifier used in base station transmitter systems (BTSs).[1] Until now, we have released over six million products. For BTSs use, the frequency is around 2 GHz. On the other hand, wireless backhaul network with millimeter wavelength is expected in near future. The frequency range for amplifier used in backhaul is 70–80 GHz due to its wide bandwidth and large capacity. However, this frequency is much higher than that of BTSs. Therefore we had to improve the operation frequency for realization of the E-band GaN HEMTs. For this purpose, we developed the process technology.

A current cutoff gain frequency*2 (f_T) is commonly used for index of RF performance. High f_T means high speed operation. f_T is expressed by the equation of $f_T = g_m / 2\pi C_{gs}$. Where, g_m and C_{gs} are transconductance and gate capacitance, respectively. From this equation, the increase in g_m and the reduction in C_{gs} are effective for the improvement in f_T. Therefore, we developed high g_m epitaxial growth technology and low C_{gs} gate process technology.

In this report, we first describe epitaxial growth technology. Then, we describe the detail of low C_{gs} gate process. We finally show the performance of GaN HEMT.

2. Epitaxial Growth Technology

Aluminum Gallium Nitride (AlGaN) is widely used for a barrier material of GaN HEMTs. High concentration two dimensional electron gas (2DEG) is generated by the band offset between AlGaN and GaN. The sheet carrier density (N_s) of 2DEG increased due to not only the spontaneous polarization effect but also the piezo polarization effect. Since g_m is strongly dependent on epi structure, the increase in N_s is effective in high g_m. However, the attainment level of AlGaN barrier is limited.

Indium Aluminum Nitride (InAlN) is also reported as the barrier material of GaN HEMTs.[2] $In_{0.17}Al_{0.83}N$ is lattice matched to GaN. The spontaneous polarization effect of this material is higher than that of AlGaN. N_s of InAlN is approximately two-fold higher compared with that of AlGaN.[3] The reduction of gate length (L_g) and a thin barrier are necessary for high speed operation. N_s is decreased in the thin AlGaN barrier. But high N_s can be obtained though the barrier is thin. So we chose InAlN for the barrier material of E-band GaN HEMTs.

InAlN has the advantages described before, but its epitaxial growth is difficult due to rough surface morphology and a large leakage current. However we overcame these problems by the development of low temperature growth technology and optimization of growth sequence in the metal-organic chemical vapor deposition (MOCVD) method.[4]

We used 4-inch of high-resistance silicon substrates. On these substrates, an AlGaN buffer layer, a GaN buffer layer, an AlN interlayer and an InAlN barrier layer were grown by the MOCVD method. A GaN cap layer is effective in reducing the gate leakage current (I_g). However, introduction of the GaN cap layer sacrifices N_s. By our optimized low temperature growth technology, we can maintain a low I_g without the GaN cap layer. Thus, we did not use the GaN cap in this

study. Despite that we used a nanometer-order thin barrier, N_s was obtained by as much as 1.5×10^{13} cm^{-2}.

3. Gate Process Technology

At first, we explain C_{gs} components. **Figure 1** shows schematic cross-sectional images of two kinds of gate structures. **Fig. 1 (a)** is a T-shaped gate structure (T-gate). C_{gs} is divided by two components. One is an intrinsic component underneath the gate. The other is a parasitic component at the gate fringe. The reduction of L_g is effective for the reduction of intrinsic components. However, when L_g becomes shorter, the parasitic component becomes relatively high and becomes dominant in total gate capacitance. The Y-shaped gate structure (Y-gate) is effective for the reduction of parasitic components. The low dielectric constant material is sandwiched between the gate fringe and epi surface, as shown in **Fig. 1 (b)**. In this study, we chose the Y-gate, because not only L_g but also L_{og} can be reduced.
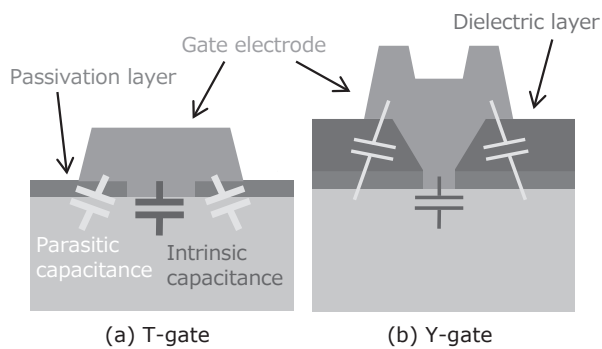

Fig. 1. Schematic cross-sectional image of two kinds of gate structure

L_g, which relates intrinsic components, is determined by lithography process at the gate opening. An i-line (365 nm) stepper is conventionally used in the lithography process. Resolution of the stepper is limited by the wavelength of the light source and numerical aperture. If we need short L_g above the resolution limit, electron beam (EB) lithography is necessary. EB lithography is suitable for formation of extreme short L_g. But this complicated process causes low yield and results in high production costs. Therefore we developed the i-line stepper based short gate process.[5]

An overview of the Y-gate process flow is shown in **Figure 2**. First, a sputtered SiN film was deposited on the surface (**Fig. 2 (a)**). Then, a photo resist (PR) pattern with approximately 300-nm-width was obtained by an i-line stepper (**Fig. 2 (b)**). The PR pattern was shrunk by an O$_2$ plasma (**Fig. 2 (c)**). Next a SiO$_2$ film was deposited on the pattern by sputtering. The SiO$_2$ film adhering to the sidewall of the PR was

removed by a buffered hydrofluoric acid (BHF) solution (**Fig. 2 (d)**). Then the PR was lifted off (**Fig. 2 (e)**).

To fabricate the ohmic contacts, a SiO$_2$ and SiN film stack needed to be removed. We took a multi-step process of reactive ion etching (RIE) and BHF in order to minimize surface damage (**Fig. 2 (f)**). The last step in ohmic contact formation is to etch the SiN film in a RIE tool. Subsequently, source and drain electrodes are formed on the InAlN barrier layer through a deposition and lift-off process, followed by a rapid thermal anneal (**Fig. 2 (g)**). In the same manner, the SiN at the base of the gate region is etched with RIE and the gate electrode was formed with evaporated metal lift-off (**Fig. 2 (h)**).

Figure 3 shows a transmission electron microscope (TEM) image of the cross section of the GaN HEMT. The
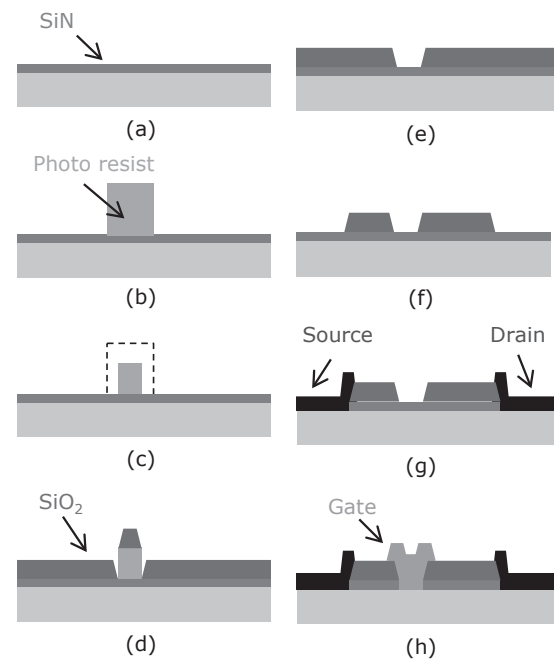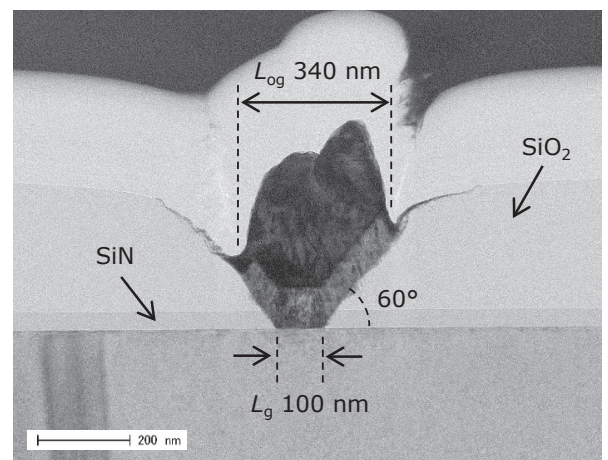

Fig. 2. Y-gate process flow

Fig. 3. Cross-sectional TEM image of gate structure

obtained values for L_g and L_{og} were extremely fine, 100 nm and 340 nm, respectively. The gate sidewall was tapered and a smooth slope shape was obtained, because we controlled SiN and SiO$_2$ to obtain the same etching rate at the gate opening etching. The angle is important, since it determines the parasitic gate capacitance and the electric field at the gate edge.[6] We controlled the angle to be 60° by optimizing the SiO$_2$-thickness and RIE conditions.

4. Evaluation

We measured the developed GaN HEMTs in three ways. First, we evaluated the DC characteristics. The evaluated device has L_g of 100 nm, L_{og} of 340 nm and gate width (W_g) of 80 × 1 µm. The drain characteristics are shown in **Figure 4**. The gate voltage (V_g) was swept from -3 to 3 V with 0.5 V steps. The maximum drain current (I_d) of 1.35 A/mm was observed. Second, the I_d-V_g and I_g-V_g characteristics were measured at V_d of 10 V as shown in **Figure 5**. Although the GaN cap was not applied, I_g of 4.9×10^{-5} A/mm at V_g of pinched-off (-5 V) was obtained. The peak g_m was as high as 550 mS/mm. This value is hardly obtained in AlGaN barrier.
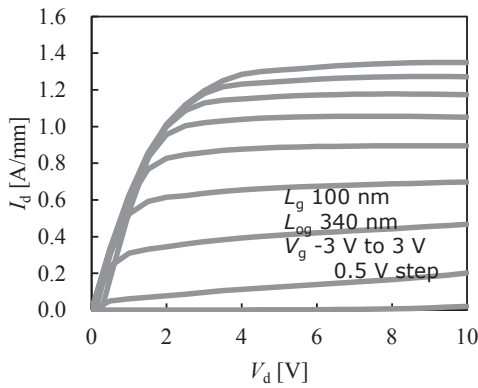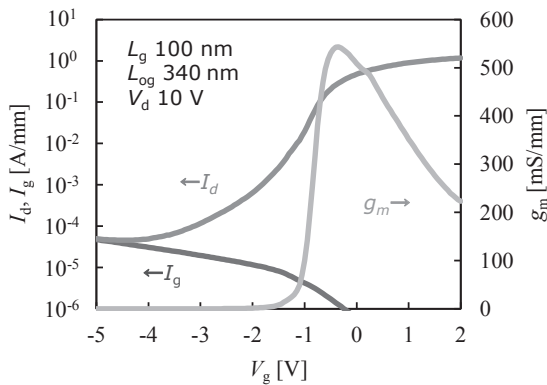
Third, we measured the S-parameters using an Agilent 8510C network analyzer for the GaN HEMTs with W_g of 50 × 2 µm from 10 to 80 GHz ranges. After the parasitic pad was de-embedded, we extracted C_{gs} and g_m from an equivalent circuit model obtained from the measured S-parameters.

L_g dependence of C_{gs} and g_m are shown in **Figure 6**. The highest g_m of 490 mS/mm was achieved at L_g of 220 nm. However, g_m decreases at L_g lower than 220 nm due to short channel effects. On the other hand, short L_g is remarkably effective in the reduction of C_{gs}. C_{gs} reduction can be seen saturated around L_g of 150 nm, because fringe capacitance became dominant in total capacitance. Next, L_{og} dependence of C_{gs} and g_m are shown in **Figure 7**. Short L_{og} is effective in the reduction of C_{gs}. From the results of **Figs. 6 and 7**, the lowest C_{gs} of 0.58 pF/mm was obtained at L_g of 100 nm and L_{og} of 340 nm.
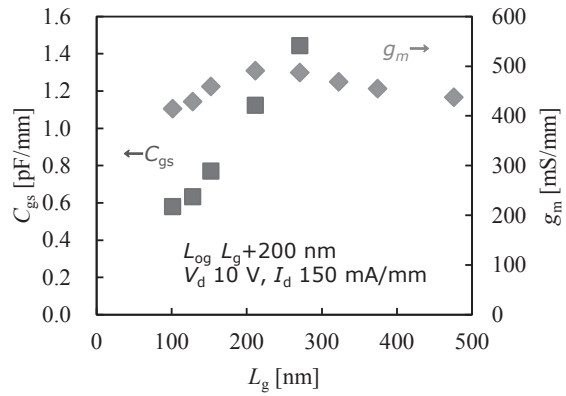
Fig. 4. I_d-V_d characteristics

Fig. 5. I_d-V_g and I_g-V_g characteristics

Fig. 6. L_g dependence of C_{gs} and g_m

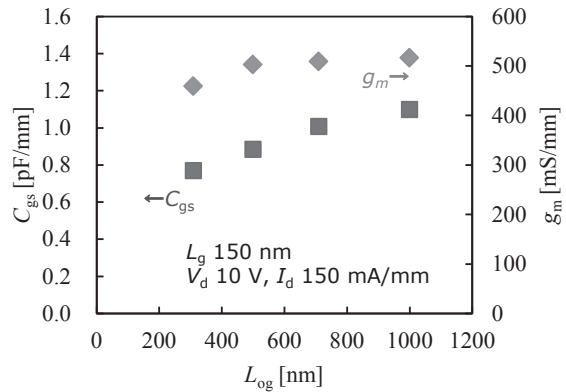**Fig. 7.** L_{og} dependence of C_{gs} and g_m

The small signal gain characteristics obtained from S parameters are shown in **Figure 8**. The evaluated device has L_g of 100 nm, L_{og} of 340 nm. f_T of 110 GHz and maximum oscillation frequency (f_{max}) of 140 GHz

were obtained under the bias condition of V_d of 10 V and I_d of 300 mA/mm. Though this f_T covers E-band wavelength, the f_{max} / f_T ratio was as low as 1.3. The reason is due to the high gate resistance by the small cross section of the gate electrode. We expect much higher f_{max} shall be achieved by introduction of the electrolytic gold plating process.
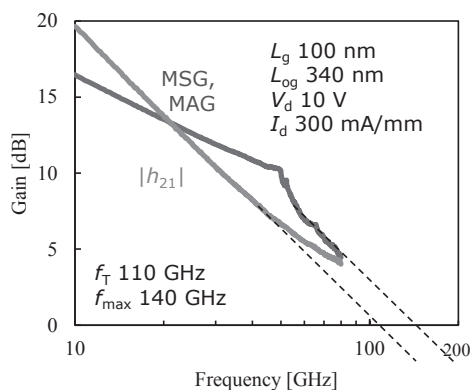

Fig. 8. Small signal gain characteristics

5. Conclusion

We improved both epitaxial growth technology and gate process technology for realization of E-band GaN HEMTs. As a result, we developed the Y-gate process with L_g of 100 nm and C_{gs} of 0.58 pF/mm. f_T was achieved at of 110 GHz. We successfully realized E-band GaN HEMTs.

Technical Terms

*1 High electron mobility transistor: One of the field effect transistors, incorporating a junction between two materials with different band gaps in the channel instead of a doped region. The channel has few collisions with impurities and is formed with high electron density.

*2 f_T: Transition frequency, an index showing the high-frequency performance of a transistor. It is also known as current gain cutoff frequency, or the gain-bandwidth product.

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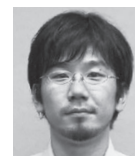**Contributors** (The lead author is indicated by an asterisk (*).)

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