

High Current SiC Transistors for Automotive Applications

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As the electrification of automobiles advances, the efficiency of power devices used for electrical power control becomes increasingly important. Although silicon (Si) power devices have been commonly used, the adoption of silicon carbide (SiC) power devices, which are more power efficient than Si devices, have been accelerating. Against this backdrop, we have focused on the development of SiC metal-oxide-semiconductor field effect transistors (MOSFETs) with trench gates for high efficiency. Our trench MOSFETs can reduce the on-resistance with the V-groove structure and achieve a high breakdown voltage due to the electric field alleviating regions implanted around the trench bottom. Here we report on our V-groove trench MOSFETs (VMOSFETs) that have a rated voltage of 1200 V and current of 200 A as required for high current automotive applications. The VMOSFETs exhibit both a low specific on-resistance of 3.4 mΩ cm² and a high breakdown voltage of 1660 V. In addition, the VMOSFETs also achieve high speed switching due to the electric field alleviating regions that reduce the parasitic capacitance.

Keywords: power device, 4H-SiC, trench MOSFET

1. Introduction

Aiming to save energy and reduce CO₂ emissions, automobile manufacturers are actively promoting the electrification of automobiles. Electric and hybrid vehicles are driven by battery-powered electric motors. Power from the batteries is controlled by power semiconductor devices (power devices). Most conventional power devices for automotive applications are silicon (Si) power devices comprising insulated gate bipolar transistors (IGBTs). To further improve the fuel efficiency of electrified automobiles, it is indispensable to reduce power loss that occurs in the power devices. Power loss consists of conduction loss and switching loss. Conduction loss is attributable to the resistance of the power device when it is turned on, while switching loss occurs when the power device is repeatedly turned on and off. Although the power device is desirable to reduce conduction loss and switching loss at the same time, the characteristics of Si IGBTs have already been enhanced to near the theoretical limit calculated from their physical properties.

As alternative materials to Si, expectations are high for silicon carbide (SiC) and gallium nitride (GaN), which are wide band gap semiconductors. Since SiC contains less crystal defects than GaN, high-quality SiC epitaxial substrates are mass-produced, and with these substrate, vertical SiC power devices can be produced. Sumitomo Electric Industries, Ltd. mass-produces 6-inch SiC epitaxial substrates named “EpiEra”.⁽¹⁾ We use a unique simulation technique to determine the doping concentration uniformity appropriate for achieving the intended device performance and yield rate. The simulation technique also ensures an extremely even film thickness and a low defect density at the same time. Since a vertical power device that uses the whole surface of the epitaxial layer, SiC is advantageous in that it achieves a high current and a high breakdown voltage range of 1200 V or more. For the above reason, SiC is expected to be used in automotive inverters that are required to achieve high power, while GaN is expected to be used in DC-DC converters that can operate on low output power. Compared with Si, SiC has a higher dielec-

tric breakdown electric field, electron saturation velocity, and thermal conductivity. Because of these outstanding features required of power devices, SiC enhances the breakdown voltage and reduces the on-resistance of the power devices. A Si power device uses an IGBT structure to achieve high breakdown voltage and low resistance at the same time. Since the Si power device depends on a bipolar operation, switching loss increases. On the other hand, the SiC metal-oxide-semiconductor field effect transistor (MOSFET) achieves a breakdown voltage equal to that of a Si power device. Thus the SiC power device ensures high-speed switching through a unipolar operation.

Two types of SiC devices – trench and planer MOSFETs – have already been commercialized in Japan and overseas. Trench MOSFETs are more effective than planer MOSFETs in increasing the cell density and thus increasing the number of channels that work as current paths. Therefore, trench MOSFETs have an advantage over planer MOSFETs in reducing power loss.

2. Features of VMOSFET

The principal feature of our V-groove trench MOSFET (VMOSFET) (see Fig. 1) is that the crystal face of the side walls of the trench/channel is {0338}.^{(2),(3)} Compared with other crystal faces, this crystal face has a high channel mobility. Thus, it significantly reduces channel resistance in conjunction with the high channel density, thereby reducing power loss.

On the other hand, a shortcoming of the trench structure is that it breaks easily when a high voltage is applied. In this state, electric field concentrates on the gate oxide film on the trench bottom (groove bottom). To enhance the reliability of the VMOSFET, we implanted p-type electric field alleviating regions (buried p-regions) around the groove bottom, thereby alleviating the electric field.⁽⁴⁾ Electrically connecting the buried p-regions to the source electrode and thus using the regions as a source potential

made it possible to reduce the parasitic capacitance (C_{rss} : feedback capacitance) between the gate drain electrodes, which affects the switching speed. An increase in switching speed also reduced power loss.⁽⁵⁾

This paper discusses the basic characteristics of the new VMOSFET that ensures a rated voltage of 1200 V and current of 200 A for automotive applications, as well as the switching characteristics of this device when it is used in an inverter.

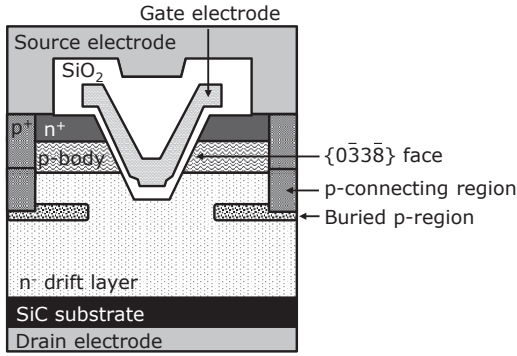


Fig. 1. Schematic Cross Section Diagram of SiC VMOSFET

3. Fabrication Method of VMOSFET

After the first SiC epitaxial layer was grown on a 150 mm n-type 4° off 4H-SiC(0001) substrate to form an n⁻ drift layer, the buried p-region was implanted by aluminum (Al) ion implantation. Following the above procedures, another n⁻ drift layer was grown in the surface layer of the substrate. The n⁺ contact region was formed by phosphorous (P) ion implantation, while the p-connecting region, p⁺ contact, and p-body regions were formed by Al ion implantation. The buried p-region was grounded after being connected to the source electrode through the p-connecting region. To form a V-groove trench structure, a thermally oxidized film was used as an etching mask. The substrate was etched thermochemically in a chlorine (Cl₂) atmosphere to bring a {0338} crystal face to the side wall of the trench.⁽⁶⁾ Subsequently, poly-Si was deposited on the trench bottom and thermally oxidized to form a 200 nm thick oxide film on the trench bottom. A gate oxide film was simultaneously formed by thermal oxidation. Subsequent to the above oxidation, the oxide interface was nitrated with nitrogen monoxide to reduce the interface state density. Polycrystalline silicon was used as the gate electrode. For the ohmic source and drain electrodes, their films were formed by sputtering and alloyed by heating to 1000°C. An Al wiring was formed on the alloy's surface.

4. Static Characteristics of VMOSFET

The I_D - V_{DS} ($V_{\text{GS}} = 3 - 18 \text{ V}$) characteristics of the new VMOSFETs are shown in Fig. 2. In on-state at room temperature, the VMOSFETs had a low specific on-resistance of 3.4 mΩ cm² ($V_{\text{GS}} = 15 \text{ V}$, $V_{\text{DS}} = 1 \text{ V}$). This figure verifies that a single die of the VMOSFETs can achieve a current of 200 A

or more. At $V_{\text{GS}} = 18 \text{ V}$, the specific on-resistance was measured to be 3.3 mΩ cm², verifying that the on-resistance does not significantly depend on the gate voltage. This means that the VMOSFET has a substantially low channel resistance. Threshold voltage V_{DS} , which is defined as the voltage at which a transistor starts functioning by flowing an electric current, was measured to be 4.0 V under a condition of $V_{\text{DS}} = 10 \text{ V}$ and $I_D = 2 \text{ mA}$. In off-state, the VMOSFETs exhibited a high breakdown voltage of 1660 V, a sufficient margin for a rated voltage of 1200 V, as shown in Fig. 3. Figure 4 shows the capacitance characteristics of the devices measured at a

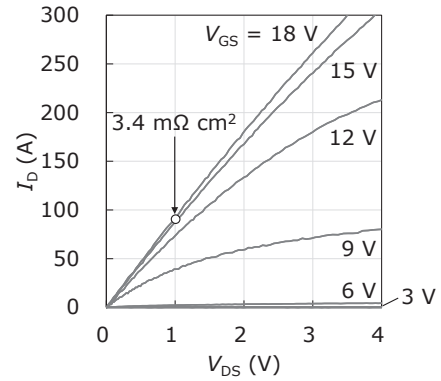


Fig. 2. I_D - V_{DS} Characteristics ($V_{\text{GS}} = 3 - 18 \text{ V}$)

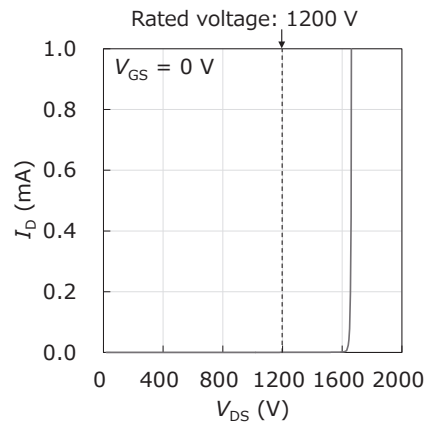


Fig. 3. I_D - V_{DS} Characteristics ($V_{\text{GS}} = 0 \text{ V}$)

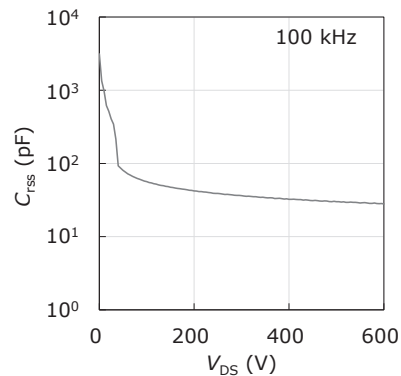


Fig. 4. Capacitance characteristics

frequency of 100 kHz.

The new VMOSFETs exhibited a low feedback capacity of 60 pF at $V_{DS} = 100$ V, verifying the effect of grounding the buried p-region. The temperature-dependence of on-resistance in a range of -55 to 175°C is shown in Fig. 5. The on-resistance was positively correlated with temperature. The probable reason for this is that the low interface state density of $\text{SiO}_2/4\text{H-SiC}\{0338\}$ minimized the change in the channel resistance and an increase in the resistance of the n^- drift layer became dominant. The temperature-dependence of threshold voltage is shown in Fig. 6. This voltage decreased linearly as the temperature increased. In particular, the threshold voltage at 175°C was 2.9 V.

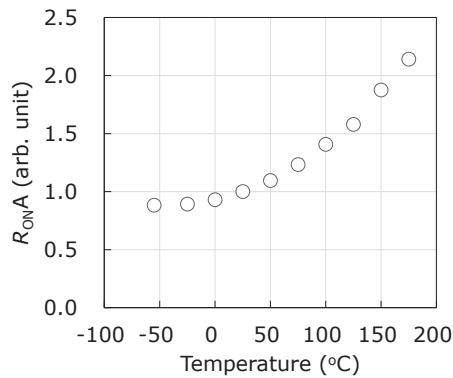


Fig. 5. Temperature-dependences of On-resistance

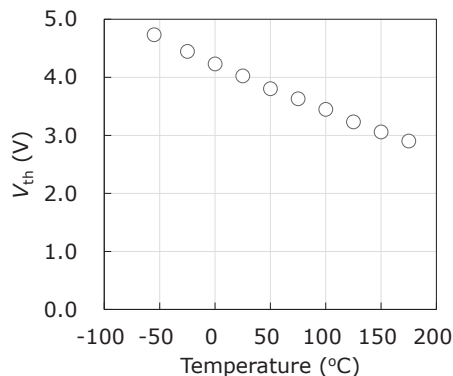


Fig. 6. Temperature-dependences of Threshold Voltage

5. Switching Characteristics of VMOSFET

Assuming that the newly developed VMOSFETs would be used to control electric motors, we evaluated the VMOSFETs with the inductive load switching circuit ($R_g = 3.3 \Omega$, $V_{GS} = +15/-5$ V, $V_{DD} = 600$ V, $I_D = 100$ A, $L = 100 \mu\text{H}$) shown in Fig. 7. The turn-on and turn-off switching waveforms are shown in Figs. 8 and 9, respectively.

As shown in Figs. 8 and 9, the new VMOSFETs switched a high current at such high speeds of 36 ns for the rise time and 12 ns for the fall time. When switching the current, the turn-on and turn-off losses of the new device were measured to be 740 μJ and 770 μJ , respectively.

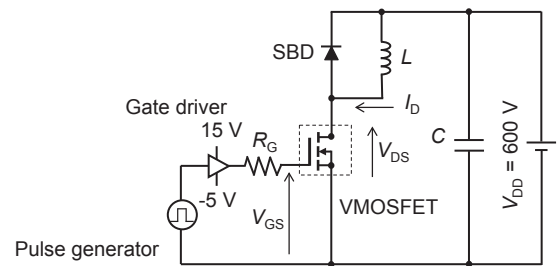


Fig. 7. Inductive Load Switching Circuit

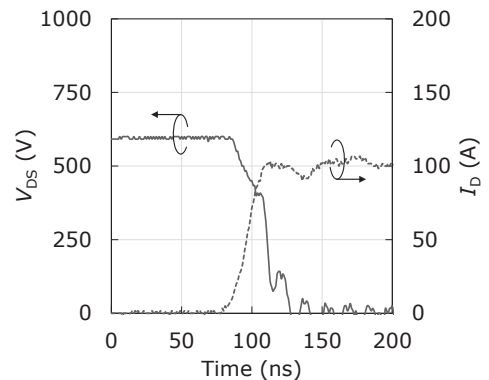


Fig. 8. Turn-on Waveform

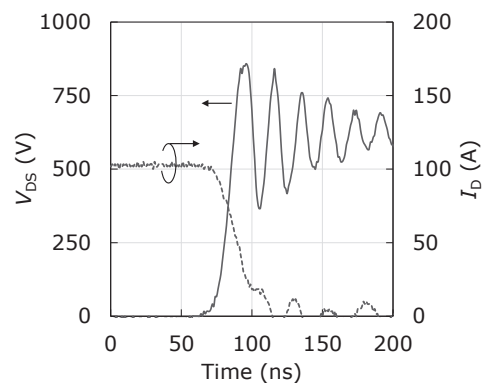


Fig. 9. Turn-off Waveform

6. Conclusion

The characteristics of the VMOSFETs we have recently developed are listed in Table 1. The new device is a V-groove trench SiC VMOSFET consisting of 4H-SiC {0338} trench side walls. Having high channel mobility, these side walls enable the device to achieve low on-resistance and high breakdown voltage at the same time. To enhance the breakdown voltage by alleviating the concentration of electric field on the V-groove trench bottom, a p-type region was implanted in the drift layer. The VMOSFETs having a rated voltage of 1200 V and current of 200 A achieves a low specific on-resistance of 3.4 $\text{m}\Omega \text{ cm}^2$ and a high breakdown voltage of 1660 V. Though a high-current element, the newly developed VMOSFETs realizes a low feedback capacitance of 60 pF. When tested using an

inductive load, the new VMOSFETs switched at a high speed. We are currently preparing for mass production of the new VMOSFETs.

Table 1. Characteristics of VMOSFETs

Item	Value	Unit	Condition
Rated current	200	A	$V_{GS} = 15 \text{ V}, T_C = 25^\circ\text{C}$
Rated voltage	1200	V	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$
On-resistance	3.4	$\text{m}\Omega \text{ cm}^2$	$V_{GS} = 15 \text{ V}, V_{DS} = 1 \text{ V}$
Threshold voltage	4.0	V	$V_{DS} = 10 \text{ V}, I_D = 2 \text{ mA}$
Breakdown voltage	1660	V	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$
Feedback capacitance	60	pF	$V_{DS} = 100 \text{ V}$
Turn-on loss	740	μJ	$R_g = 3.3 \Omega$ $V_{GS} = +15/-5 \text{ V}$ $V_{DD} = 600 \text{ V}$ $I_D = 100 \text{ A}$ $L = 100 \mu\text{H}$
Turn-off loss	770	μJ	
Rise time	36	ns	
Fall time	12	ns	

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• EpiEra is a trademark or registered trademark of Sumitomo Electric Industries, Ltd.

References

- (1) K. Wada, T. Terao, T. Miyase, T. Hori, H. Doi, and M. Furumai, "High-Quality 6-inch SiC Epitaxial Wafer "EpiEra"," SEI TECHNICAL REVIEW, No. 87, pp. 54-58 (2018)
- (2) H. Yano, T. Hirao, T. Kimoto, H. Matsunami, and H. Shiomi, "Interface properties in metal-oxide-semiconductor structures on n-type 4H-SiC (03-38)," Appl. Phys. Lett., Vol. 81, No. 25, pp. 4772-4774 (2002)
- (3) T. Hiyoshi, T. Masuda, K. Wada, S. Harada, and Y. Namikawa, "Improvement of interface state and channel mobility using 4H-SiC (0-33-8) face," Mater. Sci. Forum, Vols. 740-742, pp. 506-509 (2013)
- (4) T. Masuda, K. Wada, T. Hiyoshi, Y. Saitou, H. Tamaso, M. Sakai, K. Hiratsuka, Y. Mikamura, M. Nishiguchi, T. Hatayama, and H. Yano, "A Novel Truncated V-groove 4H-SiC MOSFET with High Avalanche Breakdown Voltage and Low Specific On-resistance," Mater. Sci. Forum, Vols. 778-780, pp. 907-910 (2014)
- (5) Y. Saitoh, T. Masuda, H. Tamaso, H. Notsu, H. Michikoshi, K. Hiratsuka, S. Harada, and Y. Mikamura, "Switching Performance of V-Groove Trench Gate SiC MOSFETs with Grounded Buried p⁺ Regions," Mater. Sci. Forum, Vols. 897, pp. 505-508 (2017)
- (6) H. Koketsu, T. Hatayama, H. Yano, and T. Fuyuki, "Shape Control of Trenched 4H-SiC C-face by Thermal Chlorine Etching," Jpn. J. Appl. Phys., Vol. 51, No. 5R, pp. 051201/1-5 (2012)

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