Development of Low-Power-Consumption IC Chipset for SFP+

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For small form-factor pluggable plus (SFP+), the authors have successfully developed chipset composed of transceiver IC equipped with Vertical-Cavity Surface-Emitting Laser (VCSEL) driver and shunt-driver IC. This paper describes the concept of low-power consumption designs and details of circuit designs. This combination of the shunt-driver and VCSEL driver with an asymmetric pre-emphasis has enabled to reduce the total power consumption of SFP+ without any degradation of optical performance. Both the transceiver IC and the shunt-driver IC can operate at 2.5V supply voltage. Consequently, the development of such IC has effectively reduced the total power consumption of SFP+ for 10GBASE-LR to 750 mW or less at operating temperature ranging from Tc = -5°C to 85°C, in accordance with the requirements of SFF-8472.

Keywords: shunt driving, VCSEL driver, SiGe-BiCMOS process, SFP+, IEEE802.3ae

1. Introduction

As one of the world's leading companies in optical transceiver business, Sumitomo Electric Industries had developed various types of optical transceiver [(1)], which were widely used in optical communication networks. We had developed LD (Laser Diode) and PD (Photo Diode) as key devices for optical communication. In addition, optical communication ICs such as LDD (Laser Diode Driver), TIA (Trans-Impedance Amplifier) and LA (Limiting Amplifier) were used in their optical transceivers such as SFF (Small Form Factor) and SFP (Small Form factor Pluggable). In particular, SFP is well-known as one of optical transceivers suitable for hot pluggable operation. These optical transceivers are mainly composed of an optical transmitter, a receiver and a controller.

In the transmitter, the LD is directly modulated by the output current of the LDD. Then optical signal is transmitted into optical fiber. For the receiver, the PD detects the optical signal and converts it into a PD current. Then the PD current is amplified by the TIA and transformed into a voltage signal. The LA amplifies the output voltage signal from the TIA and limits the signal amplitude. In addition, recent optical transceiver such as SFP has a DDM (Digital Diagnostic Monitoring) function which can monitor and manage the statuses of the transceiver. For example, LD bias current, module temperature, power supply voltage and so on. In order to achieve these functions in the small package, the authors had developed a transceiver IC which was composed of an LDD, an LIA and a DDM function, and a multi-rate TIA up to 4.25 Gbit/s operation [(2), (3)].

As the demand on data communication increased, 10 Gbit/s optical transceivers such as Transponder, XENPAK, X2 and XFP were developed. However, since these transceivers had high power consumption and large outline, the port numbers per a blade enclosure was limited. Therefore, SFP+ had been proposed by MSA (Multi Source Agreement) [(4)] so as to solve these issues.

This paper describes the design of IC chipset for SFP+ which is necessary to provide a low power solution. The chipset is composed of the shunt-driver IC and the transceiver IC in which VCSEL driver, LA, LB (Linear Buffer) and DDM are integrated. For 10GBASE-LR application, these two chips are integrated in SFP+ [(5)], and low-power consumption up to 750mW from -5°C to 85°C as module case temperature can be achieved.

2. Development of IC chipset for SFP+

Photo 1 shows the internal view of a newly developed SFP+ in which the transceiver IC and the shunt driver IC are mounted. **Figure 1** shows the block diagram of the SFP+. The main components of the SFP+ are (A) a printed circuit

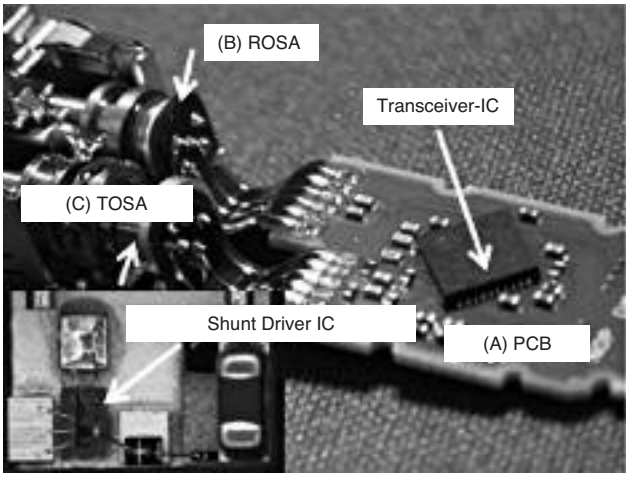


Photo 1. Internal view of a newly developed SFP+

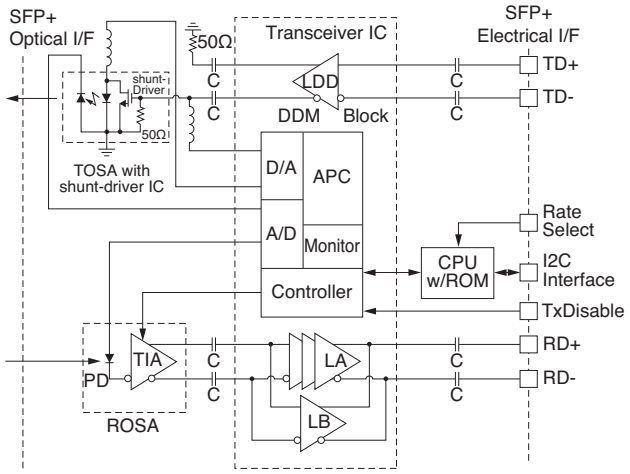


Fig. 1. Block diagram of a newly developed SFP+

board including transceiver IC and a CPU, (B) a ROSA (Receiver Optical Sub Assembly) and (C) a TOSA (Transmitter Optical Sub Assembly) in which the shunt-driver IC is mounted. The printed circuit board can be used for all applications covered by MSA.

2-1 Design concept of IC chipset

For conventional optical transceivers such as XFP or X2, the anode and cathode terminals of the edge-emitting laser diode are connected to LDD differential outputs through two coupling capacitors as shown in **Fig. 2**. In this differential driving, back termination resistance is matched with transmission line impedance. Although the low resistance (~5Ω) of the LD causes reflection from the LD, it can be entirely absorbed by the back termination resistance. As a consequence, multiple reflections between the LD and the LDD can be avoided. Additionally, the back termination resistance brings wider bandwidth with resistive loss. Using this driving technology, good eye-opening can be easily obtained but the resistive loss causes the increase in power consumption.

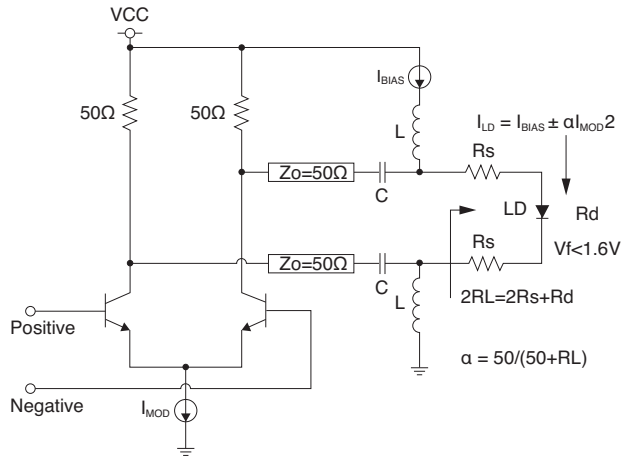


Fig. 2. Simplified circuit schematic for differential driving

Since SFP+ has good mechanical compatibility with SFP, it is considered that 48 modules can be pluged into one blade. The maximum power consumption of 1W as level-1 category is defined by MSA. Although a CDR (Clock and Data Recovery) unit is removed so as to reduce the power consumption, reducing it to 1W or less is problematic as long as the differential driving is used.

Figure 3 shows the comparison graph of power budget for each transceiver such as X2, XFP, SFP+ using differential driving and SFP+ using shunt-driving. For differential driving, the total power consumption of SFP+ is greater than 1W at Tc=85°C. In order to reduce total power consumption to 1W or less, it is necessary to reduce the power consumption of the transmitter side to 750 mW or less. Therefore, the low power solution of SFP+ has been developed, using the following technology brought by the development of IC chipset.

(1) Shunt-driver IC under 2.5V power supply
(2) VCSEL driver IC under 2.5V power supply
(3) DC/DC convertor having high efficiency

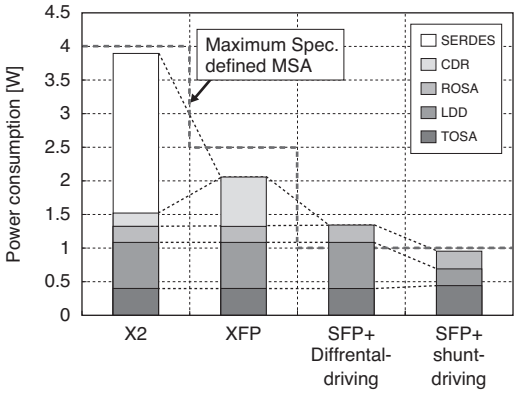


Fig. 3. Comparison graph of power budget for each transceiver

2-2 Shunt-driver IC

Shunt-driver IC, which can drive LD directly under low supply voltage, has been widely used in low speed optical communication up to 100 Mbit/s using LED (Light Emitting Diode). However, recent progress of semiconductor process technologies has changed this situation. Therefore, the shunt-driver IC to drive the LD at 10 Gbit/s has been able to be developed, using the process technologies of high speed LD and IC. The shunt-driver IC is composed of single transistor in parallel with the LD and can output modulated current to the LD. Then the LD biasing current can be subtracted from the modulated current. Eventually, the LD current can be modulated and converted to the optical signal.

Figure 4 shows the simplified circuit schematic of the optical transmitter using shunt-driving, which is composed of VCSEL driver and the shunt-driver IC. In order to enable 10 Gbit/s operations, the shunt-driver IC is mounted in TOSA and driven from the VCSEL driver IC through a 50Ω transmission line.

Since the switching transistor M1 in parallel with the LD requires high linearity, high input impedance and high speed operation, N-channel MOS-FET (Metal Oxide Semiconductor – Field Effect Transistor) with 0.18μm gate length is suitable for 10 Gbit/s operations. The gate width of M1 is decided by taking the tradeoff between speed and trans-conductance gain into account. A 50Ω termination resistor R1 is integrated in shunt-driver IC and matched with the 50Ω transmission line. The gate voltage for M1 is supplied from outside of the shunt-driver IC through a bias-T composed of L2 and C3. In order to avoid idle current due to gate voltage, the 50Ω termination is composed of R1 and C1 as AC termination. R2 is a weak pull-down resistor to prevent floating. A ferrite bead inductor L1 to prevent the leakage of high speed current is connected to the LD anode and the drain of M1.

The shunt-driver IC is tied with LD chip and TOSA package using bonding wires. As for TOSA package design, the wire length of each pin and the position of each part are optimized by electromagnetic field analysis [6]. As a consequence, the shunt-driving for 10 Gbit/s operations has been successfully developed.

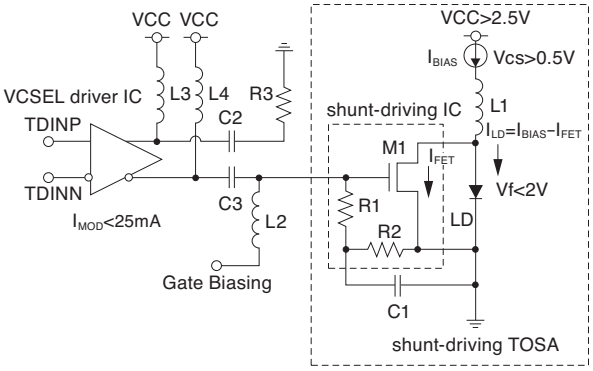


Fig. 4. Simplified circuit schematic of the optical transmitter using shunt-driving

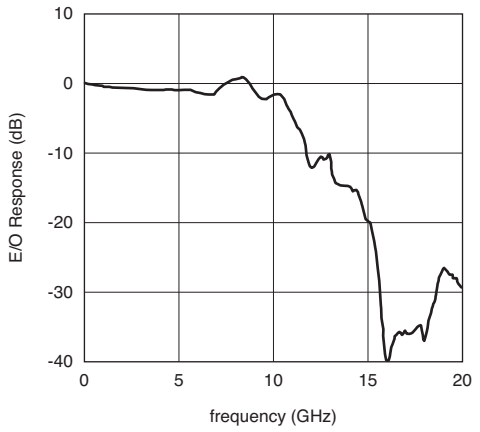


Fig. 5. E/O response of shunt-driving TOSA using in-house edge-emitting LD

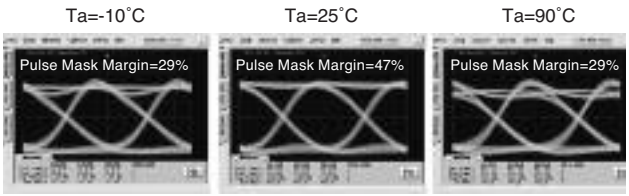


Fig.6. Optical eye-diagrams when shunt-driving TOSA is directly driven by a pulse pattern generator

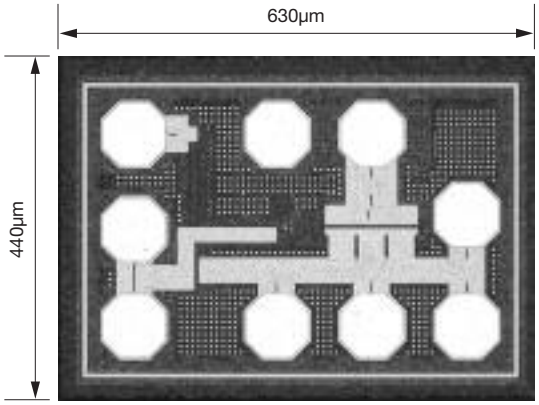


Photo 2. Chip photography of shunt-driver IC

Figure 5 shows E/O response of shunt-driving TOSA using in-house edge-emitting LD. The bandwidth of around 10GHz is enough for 10 Gbit/s operations. **Figure 6** shows the optical eye-diagram when shunt-driving TOSA is directly driven by a pulse pattern generator. Suitable mask margins of more than 20% can be achieved from -10°C to 90°C of ambient temperature.

Shunt-driving can reduce output current from VCSEL driver because M1 has trans-conductance gain gm. The output current of VCSEL driver is 2·IFET/(gm·R1), where IFET is LD modulation current, and the output impedance of VCSEL driver is perfectly matched with R1. In other words, the output current of VCSEL driver is multiplied by (gm・R1)/2. Generally, the total power consumption except for the output current tends to be higher for LDD with large drivability for edge-emitting LD, while it becomes lower for VCSEL driver with small drivability. In addition, the shunt-driving can operate under low supply voltage because it doesn't require series resistors to improve matching between driver output and LD chip. If the forward voltage of LD is less than 2.0V, 2.5V supply operation can be achieved if the current source for LD biasing can be used within 0.5V. As a consequence, low power operation can be achieved. **Photo 2** shows the chip photography of shunt-driver IC. The size of the shunt-driver IC is 440 x 630 μm, which was fabricated by a 0.18μm CMOS process with 4 metal layers.

2-3 Development of transceiver IC

Newly developed 10Gbit/s transceiver IC is composed of VCSEL driver, LA (Limiting Amplifier) to amplify the output signal from TIA, and LB (Linear Buffer)

to buffer the output signal from linear TIA. These high speed blocks occupy most of the power consumption of the transceiver IC. In order to achieve low power consumption, these high speed blocks have been designed even with a power supply under 2.5V. The DDM block in the transceiver IC can monitor transceiver statuses and alarm flag of SFP+. The analog block such as the LDD, the LA and the LB is controlled and optimized by programming internal registers. The DDM block consists of an A/D convertor and digital circuits managed by hardware state-machine. These digital circuits can operate with a 1.8V supply which is generated inside of the transceiver IC. Therefore, digital circuit size and power consumption can be efficiently reduced. **Photo 3** shows the chip photography of the transceiver IC. It is fabricated by 0.18μm SiGe-BiCMOS process (ft=80GHz, BVCE=3.6V). This chip (2.34 × 2.34 mm) is mounted in 40 pin QFN package of external dimensions 5 × 5 mm^2.

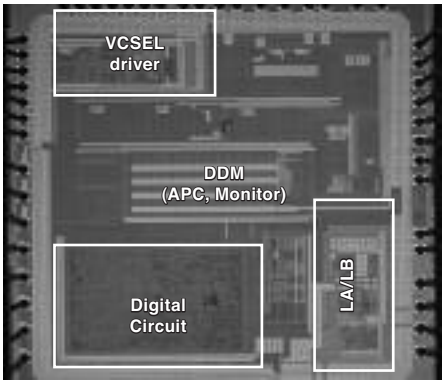


Photo 3. Chip photography of transceiver IC

(1) Development of low voltage VCSEL driver

Figure 7 shows the block diagram of VCSEL driver in the transceiver IC. The VCSEL driver is composed of an input termination circuit, an input buffer stage, a duty control stage, a pre-driver stage and a main-driver stage. The differential input signals from a host board are terminated by the input termination circuit, and then the input buffer amplifies these terminated signals. The duty-control stage can move the crossing point of the optical output by adjusting a duty control current source. Low output impedance to drive the main-driver stage can be provided by the pre-driver stage. The main-driver stage composed of CML (Current-Mode Logic) circuit can drive either the VCSEL or the shunt-driver IC in the TOSA. The output impedance of the main-driver stage is 50Ω. Pull-up inductors L3 and L4, which are connected to 2.5V supply, are needed so as to maintain voltage headroom at the output of the main-driver stage.

For the direct modulation of LD, since LD has intrinsic relaxation oscillation, the rise time of the optical signal tends to be faster than the fall time of that even if the modulation current has same rise and fall time. Therefore, it is substantially easier to create asymmetric eye-diagrams for 10Gbit/s.

An asymmetrical pre-emphasis has been developed so that asymmetrical optical waveforms can be compensated for. Generally, when a LD modulation current is directly emphasized by the pre-emphasis, the pre-emphasis consumes a lot of current because its output current is proportional to the LD modulation current. However, the combined LD driving with the shunt-driving and the VCSEL driver with asymmetric pre-emphasis can reduce total power consumption of SFP+ module without any degradation of optical performance. Because the shunt-driver with linear gain can amplify the emphasized input signal by VCSEL driver without any current consumption.

Figure 8 shows the electrical eye-diagram of VCSEL driver output. **Figure 8 (a) and 8 (b)** show the optical eye-diagrams with and without pre-emphasis, respectively. The rise/fall time without pre-emphasis is 27/22 psec, while it is 24/26 psec with pre-emphasis.

(2) Development of receiver

As the application required for SFP+, a developed receiver is necessary not only for 10GBASE-LR/SR but also for 10GBSE-LRM. For 10GBASE-LRM, the output signal from the receiver must operate in linear region so that EDC (Electric Dispersion Compensation) in the host board can compensate for the distorted signal, which is caused by the fiber dispersion that MMF (Multi-Mode Fiber) has. Although linear TIA is necessary for 10GBASE-LRM, the transceiver IC can be used for either 10GBASE-LR or -LRM, because both LA and LB are integrated in the transceiver IC and either LA or LB can be selected by programming an internal register.

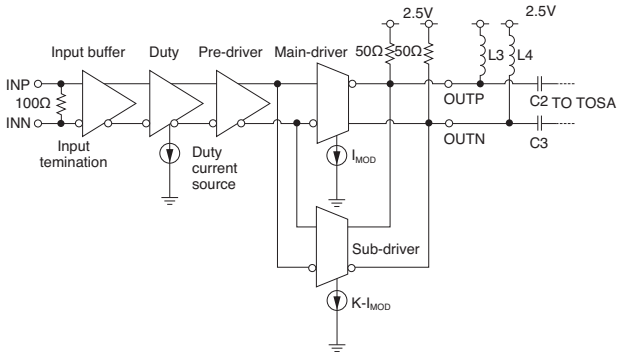
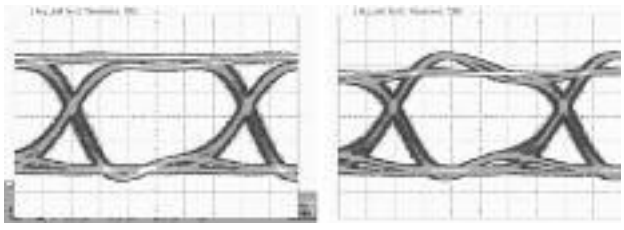


Fig. 7. Block diagram of VCSEL driver in transceiver IC



(a) w/o pre-emphasis (b) w/ pre-emphasis

Fig. 8. Electrical eye-diagrams of VCSEL driver output

LA consists of two-stage high gain blocks, a CML output buffer, an AOC (Auto Offset Controller), and a LOS (Loss Of Signal) to detect whether the signal exists or not.

Figure 9 shows the frequency dependency of the gain for both LA and LB. The bandwidth of LA is more than 10 GHz with 36 dB gain. The low cut off frequency of 100 kHz or less is decided so as to pass the stressed eye testing. The large time constant for AOC is generated by internal MIM (Metal-Insulator-Metal) capacitors. The bandwidth of LB is around 14 GHz with 2.0 dB gain. The peaking around 10 GHz is intentionally designed to compensate dielectric and resistive losses of printed circuit boards. The output resistance of CML buffer is shared with both LA and LB. Therefore, the linearity of the CML buffer is controlled by changing the trans-conductance stage for each mode.

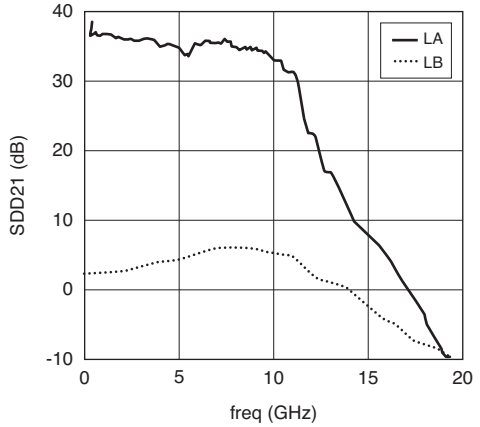


Fig. 9. Frequency dependency of the gain for LA and LB

3. Evaluation Results

SFP+ using a newly developed chipset has been developed and evaluated for 10GBASE-LR. **Figure 10** shows optical output waveforms for 10GBASE-LR. **Figure 10 (a) and (b)** show the optical waveform with and without pre-emphasis, respectively. The asymmetrical pre-emphasis can effectively compensate asymmetrical optical waveforms. **Figure 11** shows the temperature dependency of optical output waveforms from Tc= - 5°C to 85°C. **Figure 12** shows bit error ratio with and without cross-talk noise. The penalty due to the cross talk noise is around 0.5 dB. The shunt-driving

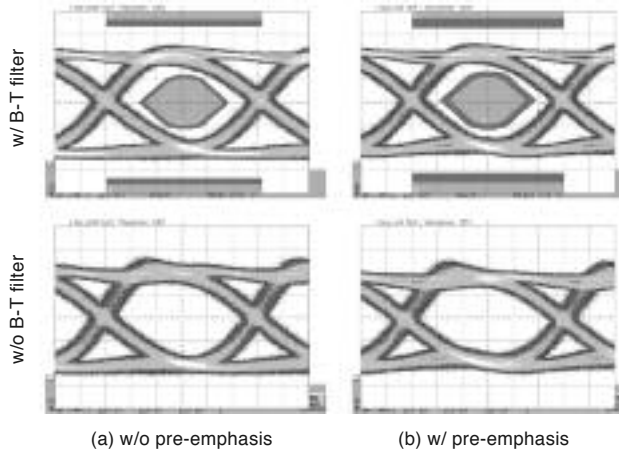


Fig. 10. Optical eye-diagrams for 10GBASE-LR

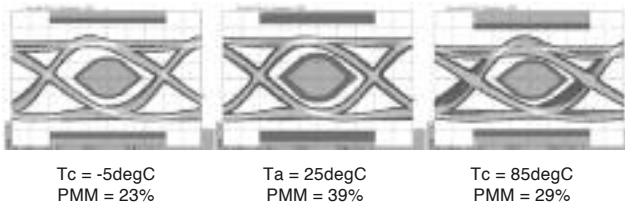


Fig. 11. Temperature dependency of optical eye-diagrams from Tc = - 5°C to 85°C.

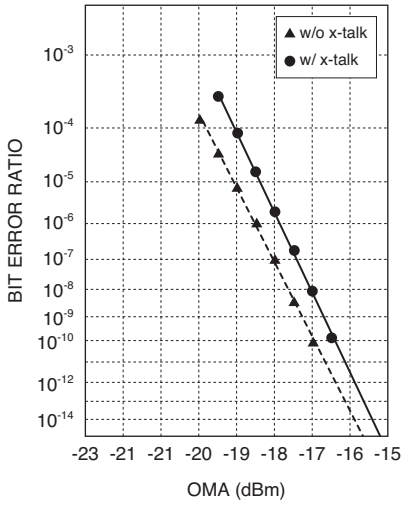


Fig. 12. Bit error ratio with and without cross-talk noise

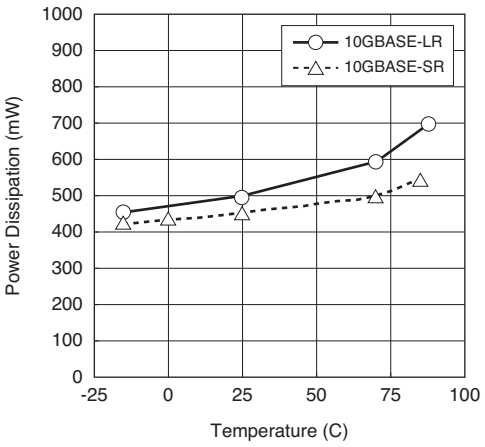


Fig. 13. Temperature dependency of power dissipation for 10GBASE-LR and -SR cases.

can reduce cross-talk noise so that the switching noise by LD modulation can be shielded by TOSA with a metal shield.

The transceiver IC can be also used for 10GBASE-SR application. **Figure 13** shows the temperature dependency of power consumption for both 10GBASE-LR and -SR. The power consumption for LR and SR at Tc=85°C is 700 mW and 550 mW, respectively. These can satisfy type-I requirement of MSA, which is 1W or less. **Figure 14** shows the temperature dependency of optical output waveforms for 10GBASE-SR.

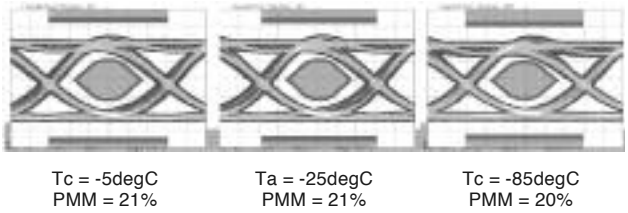


Fig. 14. Temperature dependency of optical eye-diagrams for 10GBASE-SR.

4. Conclusion

We have developed the chipset for SFP+, which is intended for 10GBASE-SR/LR/LRM applications, and confirmed excellent performance. In particular, as the strongest feature of the chipset, excellent low power design can greatly contribute to the power reduction of IT equipment.

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