SiC High Channel Mobility MOSFET

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SiC metal oxide semiconductor (MOS) devices are promising candidates for high power, high speed, and high temperature switches owing to their superior properties such as wide bandgap, high breakdown electric field, high saturation velocity and high thermal conductivity. However, the excellent device characteristics expected from these physical properties have not been realized, due to the issues related to SiO_2/SiC interface. Although several methods to improve the interface state have been reported, the issues of SiO_2/SiC interface have not been solved. In this paper, the authors improved the interface properties by using a 4H-SiC(0-33-8) face. The fabricated MOS field effect transistor (MOSFET) showed high channel mobility compared to the conventional crystal face (4H-SiC(0001)). In addition, the MOSFET showed a low on-resistance of 4 mΩ·cm^2 with a blocking voltage of 890 V.

1. Introduction

Within the context of global warming, the expectations for renewable natural energy, such as wind or solar power generation, have increased. However, natural energy is not stable and is easily influenced by weather. Furthermore, the amount of these power generations is smaller than that of traditional power generations, such as thermal and nuclear power. Thus, a high-efficiency power conversion system is strongly required to utilize these natural energies effectively. The power conversion system consists of power devices and controls electric power by switching the power devices. The inverters or converters widely used in industrial equipment also consist of power devices. Therefore, it is important for the high-efficiency power conversion system to reduce the power loss in power devices. Although almost all existing power devices have been made of silicon (Si), the efficiency of the Si power devices is approaching the theoretical limit determined by the physical properties of Si.

Silicon carbide (SiC) is a promising material for high power, high temperature, or high speed switches, owing to superior properties such as wide bandgap, high saturation velocity, high breakdown field, and high thermal conductivity[1]. The high breakdown field (ten times higher than that of Si) allows a thinner device and thus lower on-resistance. Moreover, SiC power devices can be operated at highly elevated temperatures, which enables the simplification of cooling systems. These properties fit the requirements of renewable natural energy. Since the first demonstration of SiC Schottky Barrier Diode (SBD) in 1993, SiC power devices have been developed energetically. SiC SBDs are already commercially available[2]. Recently, the SiC metal oxide semiconductor field effect transistors (MOSFETs), the ideal choice for power devices, have also been introduced in the marketplace.

In the past, SiC MOSFETs have been fabricated on 4H-SiC(0001). However, the on-resistance is much higher than the expected value because of the low channel mobility, which is due to the high interface state density (D_{it}) at the SiO_2/SiC interface. In order to reduce the D_{it}, 4H-SiC(11-20)[3] or 4H-SiC(000-1)[4] was employed and nitridation[5] or $POCl_3$ annealing[6] after the oxidation was also reported. However a fundamental solution has not been found.

As mentioned above, the selection of surface orientation strongly influences the characteristics of SiC MOSFETs. The authors selected the 4H-SiC(0-33-8) to reduce the D_{it} and to improve the channel mobility. By using the 4H-SiC(0-33-8), the D_{it} was significantly suppressed and the channel mobility was notably enhanced compare to conventional 4H-SiC(0001). In this paper, the authors report on the SiO_2/4H-SiC(0-33-8) interface properties and characteristics of the MOSFETs on 4H-SiC(0-33-8).

2. Structure and Fabrication of MOS Devices

Figure 1 shows the cross-sectional structures of the fabricated MOS devices. **Figure 1 (a)** depicts a MOS capacitor, which is a MOS device to investigate the SiO_2/SiC interface properties. **Figure 1 (b)** is a lateral MOSFET for measuring channel mobility and threshold voltage (V_{th}). **Figure 1 (c)** shows a vertical MOSFET.

The operation principle of the MOSFET is shown in **Fig. 2**. When turning on the MOSFET, gate voltage (V_G) greater than the threshold voltage should be applied to the gate electrode. This results in the formation of inversion channels, and the drain current (I_D) flows from the drain to the source electrode. On the other hand, when turning off the MOSFET, the gate voltage should be lower than the threshold voltage. In this way, the MOSFET switches to on state and off state.

The power MOSFET should be a normally-off type, which means that the MOSFET keeps the off state under the gate voltage of 0 V. The authors employed a highly doped p-well region to create the normally-off characteristics. Moreover, the authors also investigated the stability of the threshold voltage under high temperatures since SiC power devices are expected to operate safely under high
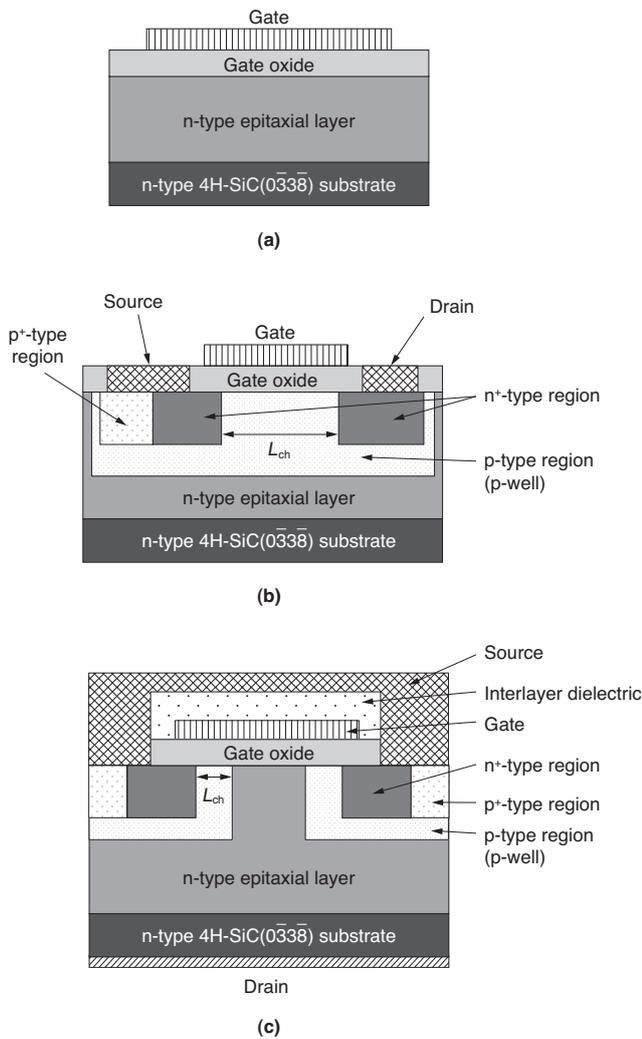
Fig. 1. MOS devices
(a) MOS capacitor, (b) lateral MOSFET, (c) vertical MOSFET.
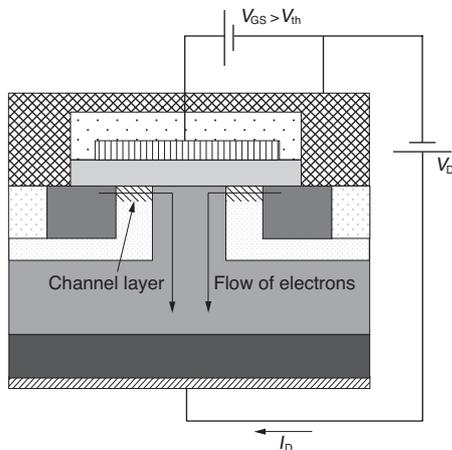
Fig. 2. Operating principle of MOSFET

temperatures.

The 4H-SiC(0-33-8) is the face tilted by 54.7° toward the <1-100> direction from the (0001) as shown in **Fig. 3**. This face corresponds to the Si(001) face (cubic structure). It is commonly known that the D_{it} of the $SiO_2/Si(001)$ interface is the lowest[7], compared to other Si faces. Similarly, the D_{it} of the $SiO_2/4H$-SiC(0-33-8) interface is expected to be the lowest value.

Epitaxial layers were grown on 4H-SiC(0-33-8) substrates by chemical vapor deposition (CVD). The thickness and doping of the epitaxial layer were 10 µm and $7 - 9 \times 10^{15}$ cm^{-3}, respectively. The p-type and n-type regions were formed by Al and P ion implantation, respectively. The concentration of the p-well region was changed from 3×10^{16} to 1×10^{18} cm^{-3} in order to control the threshold voltage. The gate oxide was formed by dry oxidation followed by nitridation[5] and Ar annealing as post oxidation annealing (POA). The thickness of the gate oxide was about 45 nm. The gate electrode was n-type poly-Si. The channel lengths (L_{ch}) of the lateral and vertical MOSFET were 100 µm and 1 µm, respectively. The vertical MOSFETs were mounted on a metal package made of CuW in order to characterize the on-resistance precisely. For comparison, the authors also fabricated the same MOS devices on 4H-SiC(0001).
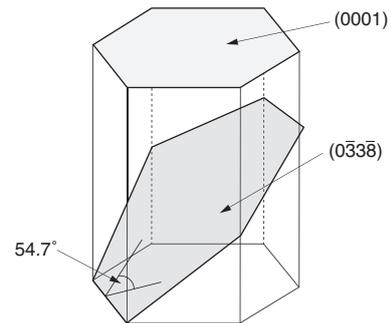
Fig. 3. 4H-SiC(0-33-8)

3. Characterization of MOS Devices

3-1 Characterization of SiO₂/SiC interface

Figure 4 shows the D_{it} distributions for MOS capacitors on (0-33-8) and (0001). The horizontal and vertical axis means the energy of the interface state (E_c: energy of the conduction band) and the D_{it}, respectively. The D_{it} was estimated by the high-low method. The high-low method is a well-known method to estimate the D_{it} by comparing the capacitance-voltage (CV) characteristics obtained with high and low frequency. The D_{it} of the $SiO_2/4H$-SiC(0-33-8) interface was notably lower than that of $SiO_2/4H$-SiC(0001). This result indicates that the channel mobility of the MOSFET on 4H-SiC(0-33-8) will be improved. (In the case that the D_{it} is low, the channel mobility tends to be high[8].)
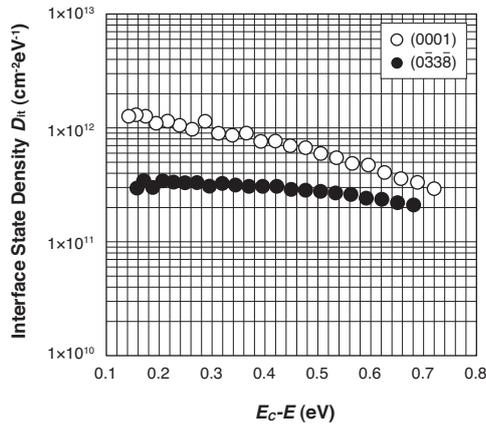
Fig. 4. The interface state density of SiO_2/SiC on (0-33-8) and (0001)

3-2 Characterization of threshold voltage and channel mobility

In this section, the authors measured the threshold voltage and estimated the channel mobility μ_{FE} (field effect mobility) by use of the lateral MOSFET (p-well: 5×10^{17} cm^{-3}) on 4H-SiC(0-33-8). The I_D-V_G characteristic and the estimated channel mobility are shown in **Fig. 5**. In spite of the highly doped p-well, the channel mobility was around 80 cm^2/Vs at a gate voltage of 15-20 V. The channel mobility obtained from the lateral MOSFET (p-well: 5×10^{17} cm^{-3}) on 4H-SiC(0001) was about 10 cm^2/Vs. It is clear that the channel mobility can be improved by using 4H-SiC(0-33-8). As mentioned above, the power MOSFET should be a normally-off type. The threshold voltage determined at the rise of the subthreshold current was 3 V.
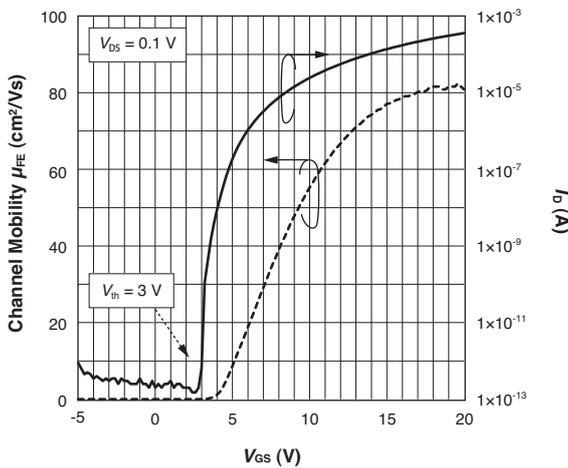
Fig. 5. The I_D-V_G characteristic of Lateral MOSFET on (0-33-8)

3-3 P-well doping dependence of threshold voltage and channel mobility

The threshold voltage should be greater than 0 V (normally-off) for the power MOSFET under its operating con-

ditions. Generally, the control of p-well doping is used to regulate the threshold voltage. (The highly doped p-well makes the threshold voltage high.) In this study, the authors investigated the p-well doping dependence of the threshold voltage and the channel mobility.

Figure 6 shows the p-well doping dependence of the threshold voltage and the channel mobility. The threshold voltage increased with increasing p-well doping. Specifically, in the case that p-well doping is greater than 5×10^{17} cm^{-3}, the threshold voltage was greater than 3 V. The channel mobility decreased with increasing p-well doping. This is because the increase of the p-well doping causes impurity scattering in the channel region. However, even though there was a highly doped p-well, the channel mobility of the 4H-SiC(0-33-8) lateral MOSFET was 60 cm^2/Vs or more. In the case of the lateral MOSFET on 4H-SiC(0001) with a p-well doping of 5×10^{17} cm^{-3}, the channel mobility decreases significantly (typical value is 10 cm^2/Vs or less[9]). This particular characteristic (the normally-off characteristic combined with the high channel mobility) is an advantage for 4H-SiC(0-33-8).
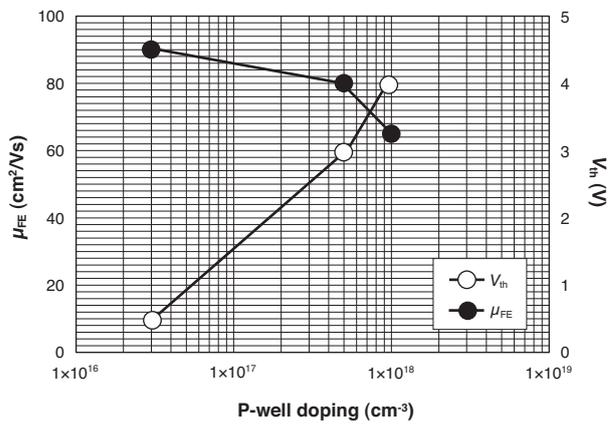
Fig. 6. The p-well doping dependence of the threshold voltage and the channel mobility
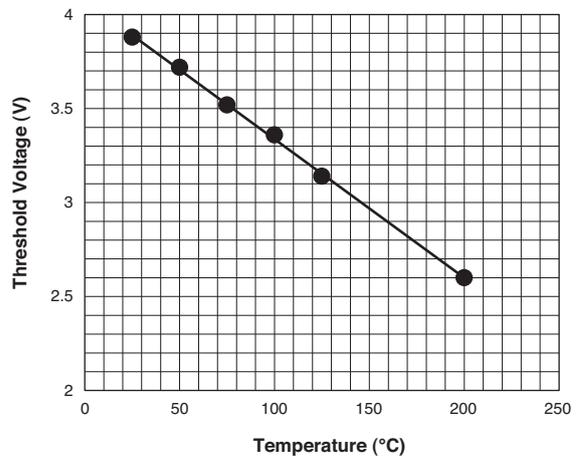
Fig. 7. The temperature dependence of the threshold voltage

Figure 7 shows the temperature dependence of the threshold voltage obtained from the 4H-SiC(0-33-8) lateral MOSFET (p-well: 1×10^{18} cm^{-3}). The threshold voltage obtained at 200°C was 2.6 V. This result means that the MOSFET can maintain the normally-off state at high temperature.

3-4 Characterization of vertical MOSFET

The authors showed superiority of the 4H-SiC(0-33-8) in the discussions above. In this section, forward and reverse characteristics of the vertical MOSFET are discussed.

Thickness and doping of the epitaxial layer used for the vertical MOSFET were 10 µm and 9×10^{15} cm^{-3}, respectively. The p-well doping was 5×10^{17} cm^{-3}. The chip size was 1.5 mm × 1.5 mm. Edge termination structure (not indicated in this paper) was employed to obtain high breakdown voltage.

Figure 8 shows the I_D-V_D characteristics of the vertical MOSFET. The gate voltage was changed from 0 V to 15 V.
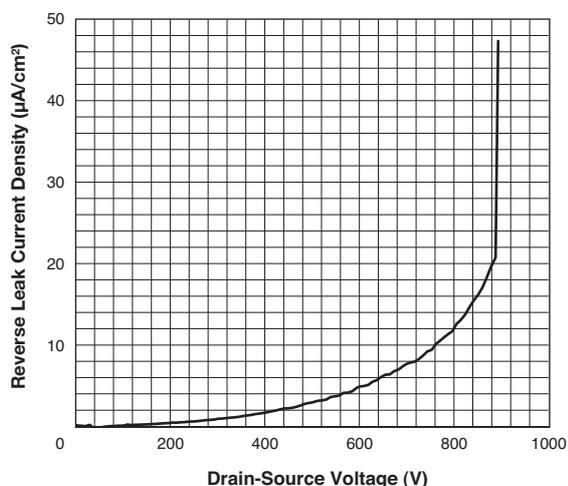
The drain current was under the detection limit at a gate voltage of 0 V (normally-off). The current density obtained at the gate voltage of 15 V and the drain voltage of 2 V was 500 A/cm^2, which means the specific on-resistance was 4 mΩ·cm^2. In the case of the vertical MOSFET on 4H-SiC(0001) with the same parameters, the specific on-resistance was 12-13 mΩ·cm^2.

Figure 9 shows the reverse characteristics of the 4H-SiC(0-33-8) vertical MOSFET. The blocking voltage was about 890 V. It is reported that the critical field of 4H-SiC(0-33-8) is lower than that of 4H-SiC(0001)[10]. The parallel-plane breakdown voltage of the epitaxial layer (doping: 9×10^{15} cm^{-3}, thickness: 10 µm) was about 1,000 V. Thus, the experimental blocking voltage was about 90% of the theoretical value.

Fig. 8. The I_D-V_D characteristics of the 4H-SiC(0-33-8) vertical MOSFET

Fig. 9. The reverse characteristics of the 4H-SiC(0-33-8) vertical MOSFET

4. Future Work

Nowadays the Si Insulated Gate Bipolar Transistor (IGBT) is mainly used in inverter applications (parallel-plane breakdown voltage: 1,200-3,300 V) such as renewable energy, electric vehicles, industrial motors, or electric railroads. High-efficiency and system downsizing are strongly desired in these applications. Therefore, the properties of SiC MOSFETs open up many possibilities for solving these problems. It is an indubitable fact that the efficiency of the power systems can be improved by replacing the existing Si power devices with the SiC MOSFETs. Moreover, as mentioned in the discussions above, the 4H-SiC(0-33-8) allows high efficiency compared to the conventional 4H-SiC(0001). In addition, the MOSFET on 4H-SiC(0-33-8) showed stable operation and normally-off state even at high temperatures. It means that cooling systems can be simplified and downsized.

In future work, the authors will optimize the structure and fabrication processes of the MOSFET on 4H-SiC(0-33-8). The expansion of the chip size and current density (low on-resistance) are also important tasks because the inverters and converters require a high current. Furthermore, high breakdown voltages greater than 3,300 V are necessary for electric railroads or electric transmission. In order to respond to these demands, the authors will work to increase the breakdown voltage by increasing the thickness of the epitaxial layer and optimizing the edge termination structure. The authors are also exploring the new applications that are made possible by the use of SiC power devices.

5. Conclusion

The electrical properties of the SiO$_2$/SiC interface were dramatically improved by using 4H-SiC(0-33-8). The MOSFET (p-well: 5×10^{17} cm^{-3}) showed a high channel mobility of 80 cm^2/Vs and a threshold voltage of 3 V. In addition, the MOSFET demonstrated stable operation at 200°C. Furthermore, the authors achieved the on-resistance of 4 mΩ·cm^2 and the blocking voltage of 890 V.

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