4H-SiC V-Groove Trench MOSFETs with the Buried p+ Regions

Yu SAITOH*, Toru HIYOSHI, Keiji WADA, Takeyoshi MASUDA, Takashi TSUNO and Yasuki MIKAMURA

We have been developing a metal-oxide-semiconductor field effect transistor (MOSFET) that has a V-groove shaped trench structure. Forming a 4H-SiC {0$\bar{3}\bar{3}$8} facet by thermochemical etching followed by thermal oxidation on the channel region of a trench MOSFET, we obtained low on-resistance because of excellent MOS interface characteristics. Furthermore, we introduced an electric field concentration layer with a p^+ type buried region into a drift layer in order to raise high breakdown voltage, suppressing gate insulation film breakdown in the trench bottom. Specific on-resistance and breakdown voltage of the trench MOSFET were measured to be 3.5 mΩcm^2 (V_{GS} = 18 V, V_{DS} = 1 V) and 1,700 V, respectively. The introduction of the optimized p^+ type buried region improved the breakdown voltage of the trench MOSFETs, and no performance degradation in the specific on-resistance and in the switching capability was confirmed. The typical turn-on and turn-off switching time for the resistive load switching characteristic were estimated to be 92 ns and 27 ns, respectively, at a drain voltage of 600 V. We also tested the stability of threshold voltage in the trench MOSFETs.

Keywords: 4H-SiC, power device, trench MOSFET

1. Introduction

In recent years, the need for reduction in carbon dioxide emissions has been recognized widely because of growing international concern about global warming. In addition, high efficiency use of electric energy and the introduction of renewable energy by the construction of a smart grid has attracted attention in Japan following the Fukushima Dai-ichi nuclear power plant accident.

The technology of power semiconductor devices for transmitting and using generated electric energy efficiently is called power electronics. The main portion of the generated electric energy is consumed after undergoing several transformations, many of them carried out by power electronic converters. In addition, the largest portions of the power losses in these power electronic converters are dissipated in their power semiconductor devices. The present semiconductor power devices such as metal oxide semiconductor field effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs), are basically made of silicon (Si). Though the devices have been developed by structural modification with microfabrication based on the mature Si LSI technology, it is impossible to overcome the material limits of Si. The use of these new power semiconductor devices will allow increasing the efficiency of the electric energy transformations achieving a more rational usage of the electric energy. Therefore, it is strongly expected that power devices will be developed using new materials that exceed the limits of Si.

Silicon carbide (SiC), metal oxide semiconductor (MOS) devices are promising candidates for high power, high speed, and high temperature switches owing to their superior properties such as wide bandgap, high breakdown electric field, high saturation velocity and high thermal conductivity (**Table 1**). The high thermal conductivity of SiC is a great advantage in comparison with Si devices since it allows to operate at higher current density ratings as well as to minimize the size of the cooling systems. The development of SiC power devices for high switching speed and for low on-state losses has been carried out energetically in order to utilize these material characteristics[1]. However, the very low inversion channel mobility obtained on 4H-SiC (0001) has prevented for many years the fabrication of low-resistance MOSFETs. The use of nitrogen during post-oxidation annealing and the formation of the MOS channel on alternative crystal faces with smoothing surface morphology have emerged as being effective in reducing the density of interface traps (D_{it}), and in improving the quality of the MOS interface.

Recently, a SiC double implanted MOSFETs (DiMOSFETs) of a planar structure fabricated on a 4H-SiC (0001) face have been introduced in the marketplace[2, 3]. Furthermore, the trench structure MOSFETs are advantageous for reducing energy loss because of no JFET region resistance peculiar to the DiMOSFETs and are becoming the mainstream of the development

Table 1. Properties of semiconductors

	Si	4H-SiC	6H-SiC
Bandgap [eV]	1.12	3.26	3.02
Electric breakdown field [MV cm^{-1}]	0.3	2.8	3.0
Electron mobility [cm^2 V^{-1} s^{-1}]	1,350	1,000	460
Saturated electron drift velocity [10^{7}cm s^{-1}]	1.0	2.2	1.9
Thermal conductivity [W cm^{-1} K^{-1}]	1.5	4.9	4.9

of SiC MOSFETs.

We have developed V-groove SiC trench MOSFETs which are characterized by a gate structure which consists of {0$\bar{3}$3$\bar{8}$} facets[4]-[7]. The MOS structure fabricated on {0$\bar{3}$3$\bar{8}$} facets can reduce channel resistance compared to the DiMOSFET because of higher channel mobility owing to lower D_{it}. However, an electric field tends to concentrate on the gate oxide at the trench bottom under high source-drain bias, and induce oxide breakdown at the trench bottom due to the breakdown strength of SiC that is 10 times higher than that of Si. In order to achieve both a high breakdown voltage and a low on-resistance simultaneously, we introduced an electric field concentration layer with p-type buried region into a drift layer for suppressing gate insulation film breakdown at the trench bottom. We will report basic characteristics and switching characteristics of the V-groove SiC MOSFET with the p-type buried structure and inspect the utility in power electronic converter use.

2. Structure and Fabrication of MOS Devices

Figure 1 shows the schematic cross-sectional view of the 4H-SiC trench MOSFET with p^+ buried region below the trench bottom. The SiC epitaxial layer was grown on 4˚off-axis n-type 4H-SiC (000$\bar{1}$) substrate by chemical vapor deposition. The doping concentration and thickness of the epitaxial layer were 4.5×10^{15} cm^{-3} and 12 µm, respectively. The p^+ regions were formed by aluminum (Al) ion implantation. Then, the second epitaxial layer was grown with a doping concentration of 7.0×10^{15} cm^{-3} and a thickness of 3 µm. The n^+, p^+ and p-body region were formed by phosphorus and Al ion implantation. The channel length is 0.6 µm along the trench sidewall. Subsequently, V-groove trench structures were formed by the thermochemical self-organized etching process in chlorine ambient after the silicon dioxide (SiO_2) etching mask fabrication[8]. **Figure 2** shows the scanning electron microscopic image of the V-groove trench structure after the etching, showing quite smooth sidewall and bottom without sub-trench causing degradation in breakdown voltage. Gate oxide was thermally grown, followed by nitridation and post oxidation annealing, resulting in an oxide thickness about 50 nm. The poly-Si gate electrode was deposited and patterned. The source and drain contact metal were fabricated and alloyed at the temperature of 1,000˚C. An Al electrode was deposited on the alloyed contact metal.

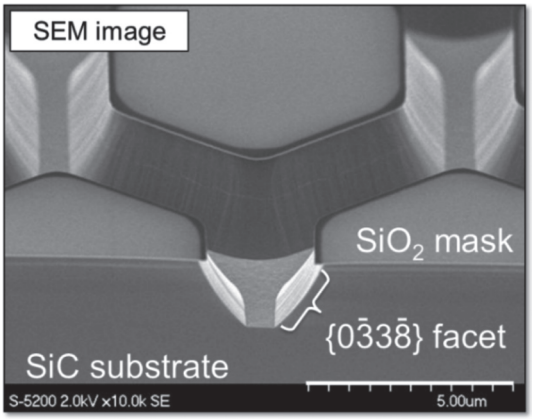

Fig. 2. A scanning electron microscopic image of 4H-SiC after V-groove etching process

3. Characterization of MOS Devices

Figure 3 shows the on-state forward I_D-V_{DS} characteristics of the V-groove SiC MOSFET. The specific on-resistance with respect to the active area size is estimated to be 3.5 mΩcm^2 (V_{GS} = 18 V, V_{DS} = 1 V) at room temperature.

Figure 4 shows the device simulation results in on-state current density distributions for the trench MOSFETs both with and without buried p^+ regions. The current density distributions were calculated by Atlas™

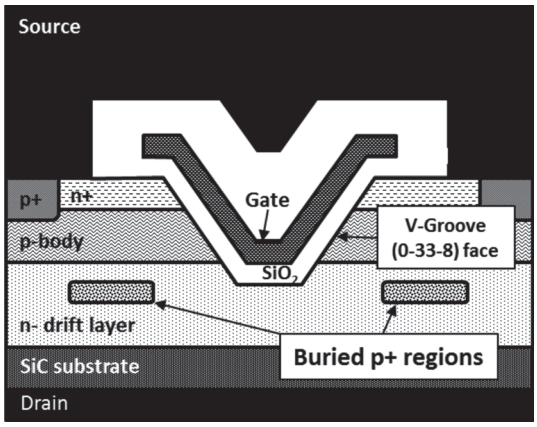

Fig. 1. Schematic structure of a 4H-SiC V-groove trench MOSFET with buried p^+ region

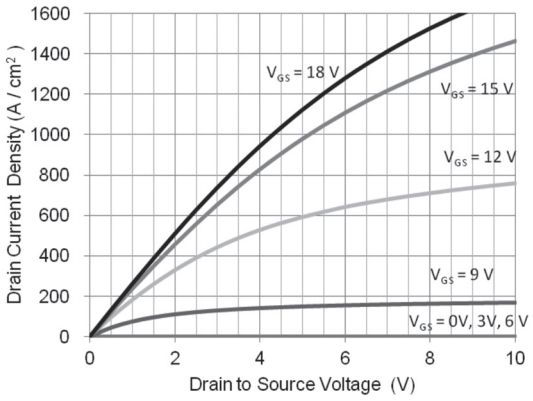

Fig. 3. On-state static characteristics of the trench MOSFET

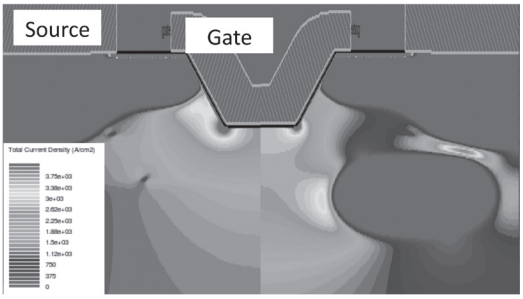

Fig. 4. Device simulation results of the on-state current distributions for the trench MOSFETs both with and without buried p⁺ region

of Silvaco TCAD. The current distribution of the trench MOSFET with a p⁺ region is shown on the right side of **Fig. 4**. Even though the current has to flow avoiding the buried p⁺ region, total current reduction compared to without a p⁺ region device is small since the aperture of the p⁺ region exists under the trench bottom where current density becomes highest. The calculated specific on-resistances of the MOSFETs with and without a p⁺ region are estimated to be 3.6 mΩcm² and 3.1 mΩcm², respectively, as the simulation results are shown in **Fig. 5**.

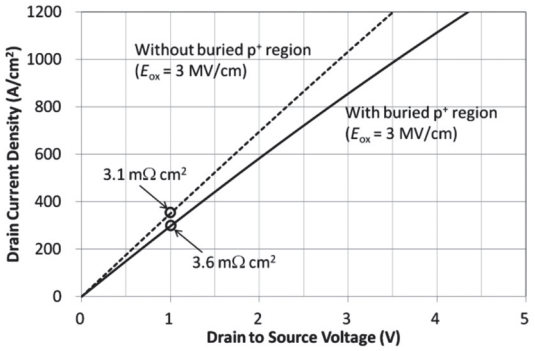

Fig. 5. Calculated I_D-V_{DS} characteristics of the trench MOSFETs for both with and without buried p⁺ region

Blocking characteristics of the trench MOSFET are shown in **Fig. 6**. The trench MOSFET with buried p⁺ regions demonstrates the blocking capability of 1,700 V as avalanche breakdown at room temperature. On the other hand, a breakdown voltage for the trench MOSFET without buried p⁺ regions is approximately 575 V, generating the gate oxide break at the trench bottom. The MOSFETs with the buried p⁺ regions showed the higher breakdown voltage, indicating that the p⁺ regions alleviate the electric field crowding at the trench bottom. **Figure 7** shows the electric field distributions at the drain voltage of 1,200 V, which is calculated by device simulation for the trench MOSFETs both with and

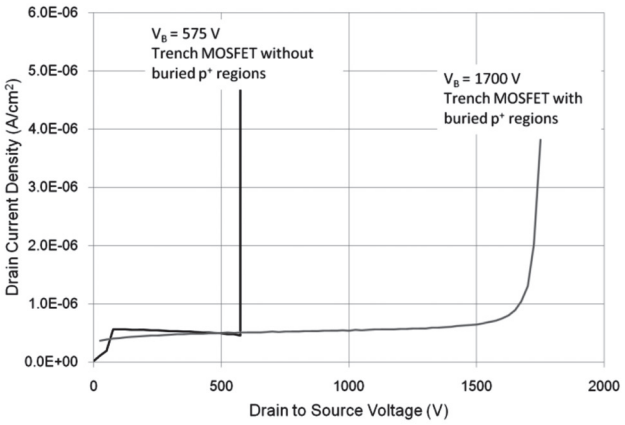

Fig. 6. Blocking characteristics of the trench MOSFETs with and without buried p⁺ regions

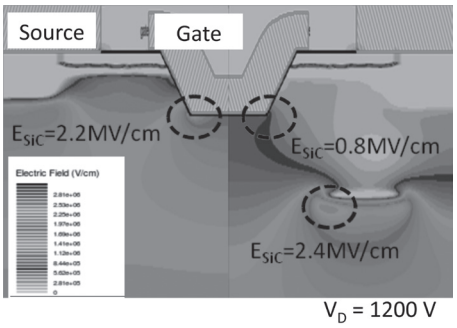

Fig. 7. Device simulation results of Electric field distributions of the trench MOSFETs with and without p⁺ region at the drain voltage of 1,200 V

without a p⁺ region. The highest electric field point in SiC can be removed from the trench bottom to the p⁺ region, dramatically alleviating the gate oxide electric field.

Switching performance of the V-groove trench MOSFETs along with a resistive load was investigated in turn-on and turn-off characteristics. The switching setup circuit is shown in **Fig. 8**. Switching measurements were carried out for both MOSFETs with and without buried p⁺ regions in order to bring out the effect of the floating p⁺ regions in the drift region. The chip size of the MOSFETs used in the dynamic measurement was 3 × 3 mm². **Figure 9** shows the switching characteristics for the trench MOSFET with p⁺ regions at a drain voltage of 600 V with a load resistor of 22Ω in order to obtain a drain current of 27 A while switching. The external gate resistance, R_G was 4.7Ω. Switching waveforms of turn-on and turn-off are shown in **Figs. 9 and 10**, respectively. From the measured wave forms, excellent turn-on and turn-off switching properties can be seen in the trench MOSFETs with buried p⁺ regions. Typical switching time and energy in turn-on and turn-off operations are estimated to be t_r = 92 ns, E_{on} = 252 μJ and t_f = 27 ns, E_{off} = 164 μJ, respectively.

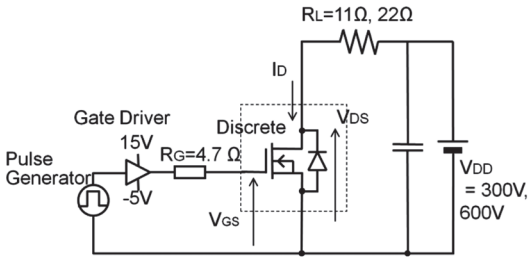

Fig. 8. Resistive load switching setup

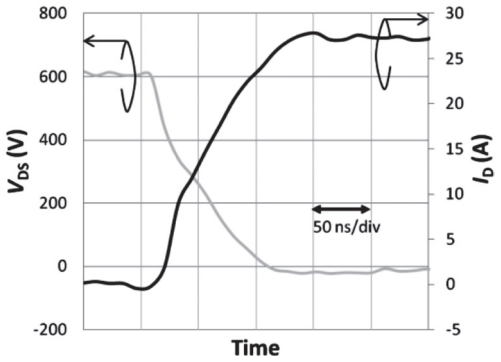

Fig. 9. Output turn-on waveforms at a V_{DS} of 600 V switching for the trench MOSFET with p⁺ regions (t_r = 92 ns, E_{on} = 252 µJ)

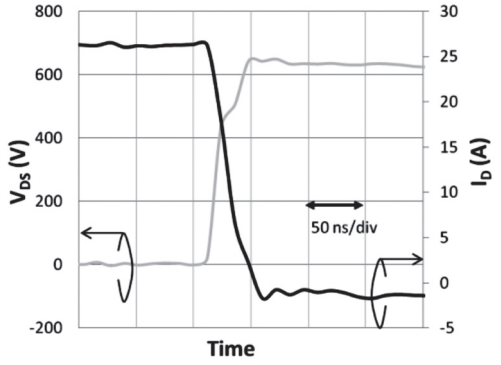

Fig. 10. Output turn-off waveforms at a V_{DS} of 600 V switching for the trench MOSFET with p⁺ regions (t_f = 27 ns, E_{off} = 164 µJ)

Meanwhile, switching characteristics of the trench MOSFET without buried p⁺ regions were also checked to examine the influence of the buried p⁺ region by using the same switching setup at a lower drain voltage of 300 V because of the lower blocking capability in the MOSFET without p⁺ region as pointed out in **Figs 11 and 12**. From the measurements for both trench MOSFETs with and without p⁺ regions, turn-on switching time and energy are estimated to be t_r = 76 ns, E_{on} = 89 µJ and t_r = 97 ns, E_{on} = 108 µJ, respectively.

On the other hand, from the turn-off waveforms, turn-off switching time and energy are estimated to be

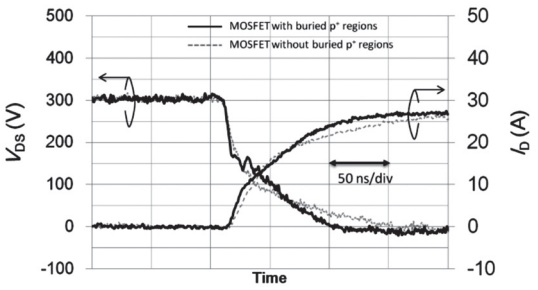

Fig. 11. Output turn-on waveforms at a V_{DS} of 300 V switching for the trench MOSFETs with and without p⁺ regions

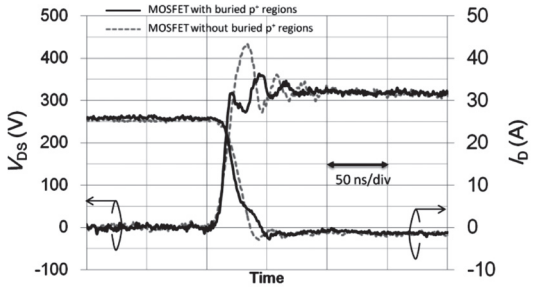

Fig. 12. Output turn-off waveforms at a V_{DS} of 300 V switching for the trench MOSFETs with and without p⁺ regions

t_f = 9.8 ns, E_{off} = 85 µJ and t_f = 14 ns, E_{off} = 86.2 µJ, respectively. As a comparison result of the switching measurement on both of the trench MOSFETs, dynamic characteristics of the trench MOSFET with buried p⁺ regions have almost equivalent or higher switching performance compared to the MOSFET without p⁺ regions. These dynamic performances of the trench MOSFETs have revealed that the structurally well-designed buried p⁺ regions haven't negatively affected the switching characteristics.

The V_{th} stability is an important issue for SiC MOS devices. We tested the V_{th} stability of the trench MOSFETs in both the positive and the negative gate bias conditions at high temperature (175˚C). **Figure 13 and Figure 14** show the time dependence of the V_{th}

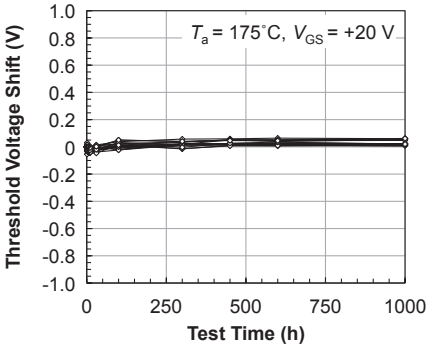

Fig. 13. Time dependences of V_{th} shift of positive gate bias at 175˚C (n=3)

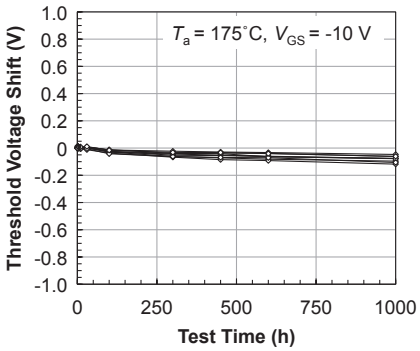

Fig. 14. Time dependences of V_{th} shift of negative gate bias stress at 175˚C (n=3)

shift (ΔV_{th}). The V_{th} was almost constant after the both the positive and negative gate bias stress at high temperature for 1,000 hours. The SiC MOS devices on (0001) or (000$\bar{1}$) are well known for the V_{th} shift due to the interface traps[9]. We consider that the V_{th} stability of the trench MOSFETs is derived from the low trap density at the SiO_2/{03$\bar{3}$8$\bar{}$} interfaces.

4. Future Work

Semiconductor devices with a blocking voltage of 600-1700 V are widely used in various power electronics applications, such as photovoltaic power generation power conditioners, inverters for hybrid cars and industrial motors, and the market size is growing. Nowadays, the Si IGBT is mainly used in the inverter applications, and the cost reduction at the same level as the Si devices is essential for substituting SiC devices for silicon ones. Reduction of the specific on-resistance enables us to reduce the number of devices per current capacity, and as a result can lower the material cost of SiC. Thinning the thickness of the drift layer, which occupies about 1/3 of the device resistance, or increasing the carrier concentration of that layer, is effective for lowering the specific on-resistance of the V-groove SiC MOSFET. However, lowering the specific on-resistance, at the same time, induces degradation of the breakdown voltage because of higher electric field concentration at the trench bottom. In future work, we will optimize the buried p^+ type regions also in order to solve this problem.

5. Conclusion

We reported the static and switching properties of the V-groove SiC MOSFET fabricated on the 4H-SiC (000$\bar{1}$) substrate. We developed V-groove SiC trench MOSFETs which have the channel regions consisting of 4H-SiC {03$\bar{3}$8$\bar{}$} facets formed by novel thermochemical etching, and obtained low specific on-resistance because of excellent MOS interface characteristics. Furthermore, we introduced an electric field concentration layer with buried p^+ type regions into the drift layer in order to suppress gate insulation film breakdown at the trench bottom. Measured values of both specific on-resistance and breakdown voltage of the V-groove SiC MOSFETs were 3.5 mΩcm^2 (V_{GS} = 18 V, V_{DS} = 1 V) and 1,700 V, respectively. The switching capability of the V-groove SiC MOSFETs demonstrated almost the same fast dynamic characteristics as the MOSFETs that have no buried p^+ type region and no performance degradation was confirmed due to the introduction of the buried p^+ type region. We also tested the stability of threshold voltage in the trench MOSFETs. Although the V_{th} of MOS devices on (0001) tends to shift, that of the V-groove SiC MOSFETs was almost constant for 1,000 hours. We consider that the V_{th} stability of the trench MOSFETs is derived from the low trap density at the SiO_2/{03$\bar{3}$8$\bar{}$} interfaces.

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