Application of Chip Formation Simulation to Development of Cutting Tools

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The simulation of chip formation processes was started as a method to construct cutting theories or understand cutting phenomena and has recently been used for actual applications. On the other hand, it is still difficult to simulate all cutting processes with sufficient accuracy because cutting processes are conducted under high temperatures and pressures at high deformation speeds. In this paper, we explain the history of the chip formation simulation and its application examples for cutting tool development. We also discuss what to consider when using the simulation.

Keywords: chip, simulation, finite element method

1. Introduction

Cutting is a machining technique with a long history. Although its use in the industrial sector advanced early, efforts to theorize cutting emerged lately in the 20th century. Of such efforts, simulations of chip formation processes began as a means of formulating cutting theories or understanding the phenomena involved in cutting. As such, for some time after its emergence, simulation remained confined to use only for academic purposes. However, the industrial sector's expectations gradually rose for the application of simulation to practical cutting, as in the cases of other machining techniques. In recent years, realistic and practical simulation techniques have been developed and increasingly used in cutting condition setting and tool development. Sumitomo Electric Industries, Ltd. began to look at this matter in the 1990s and has used chip formation simulations to develop cutting tools since 2000. This paper reports on how chip formation simulations evolved, along with Sumitomo Electric's approach and application examples. It also refers to future developments and tasks in this area.

Depending on simulation techniques and developments, chip formation simulations can be classified into four groups: (1) Pushing analysis, (2) Steady-state analysis, (3) Transition process analysis, and (4) Three-dimensional analysis, as shown in Fig. 1.[(2)] Pushing analysis (1) determines the extent of the plastic region and the pressure distribution on the tool surface, rendering a rigid-body displacement to a shape that represents how the chip flows, up to the point of time when a steady state is reached.[(3),(4)] Using this technique, it is possible to roughly explain the mechanical state of the regions close to the cutting edge. However, concerning accuracy, pushing analysis is inadequate, with the results largely depending on the initial model. For steady-state analysis (2), several methods are used. One representative method, developed by Shirakashi et al. and known as the iterative convergence method,[(5)] repeats elastic-plastic calculation and corrections in shearing angle and other settings. This method is only applicable to steady-state cutting processes. However, it is advantageous in determining steady-state solutions usually within a relatively short period of time.

2. Development Process of Chip Formation Simulation

2-1 Development of simulation models

Theorization of phenomena involved in chip formation observed in cutting advanced on the basis of shear angle theory.[(1)] However, it was still difficult for analytical techniques to produce solutions with adequate accuracy, because chip formation is a phenomenon in which the work material deforms at a high rate under high-temperature and high-pressure conditions, involving many nonlinear phenomena. As a solution to this difficulty, in around 1970, numerical analysis techniques including the finite element method (FEM)*1 began to be applied to chip formation processes, because such techniques enable determination of numerical solutions even for nonlinear phenomena, such as mentioned above, and are also beneficial in terms of theorization.

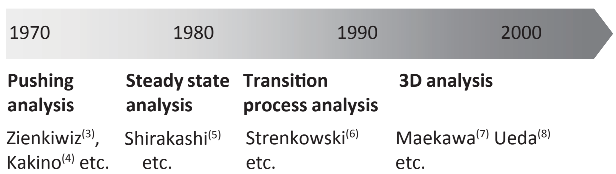


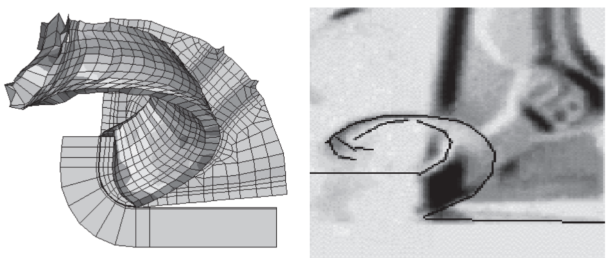
Fig. 1. Developments of simulation techniques

In the middle of the 1980s, owing to the evolution of computers, it became possible to conduct transition process analyses (3) of states spanning the initial cutting stage to the steady-state stage. Strenkowski et al.[(6)] conducted FEM analysis of a workpiece, as an elastic-perfectly plastic solid, and a tool, as an elastic solid, from the initial state to steady-state cutting to describe chip curl formation. Thereafter, in general, this transition process analysis became prevalent in research efforts, which was then followed by more realistic three-dimensional analyses (3).[7],[8] In the late 1990s, commercial software tailored to chip formation simulation appeared on the market, the use of which gradually spread in the industrial sector.

Incidentally, aside from FEM simulations, analyses using the molecular dynamics method have also been conducted, assuming ultra-fine atomic-level machining.[9]

2-2 Sumitomo Electric's approach

Sumitomo Electric began to work on developing chip formation simulation in the 1990s specifically with the development of a chip breaker for chip treatment in mind. Conducting a joint industry/academia research project,[10] the company developed a practical simulation technique[11] around 2000. Figure 2 shows an example simulation of chip formation in turning. The simulation accurately depicted the chip geometry and the cutting force. The simulation results were used to refine candidate prototype geometry, fabricate a die, and develop and commercialize the finishing chip breaker Type LU.



(a) Simulation results (b) High-speed video image

Fig. 2. Chip formation in turning [11]
(S15C, vc=200m/min, f=0.2mm/rev, ap=1.5mm)

Using these Sumitomo Electric's proprietary techniques and introducing the aforementioned commercial software AdvantEdge designed specifically for chip formation simulation, which comes with a database of more than 100 workpiece types, we provide technical support, termed by Sumitomo Electric "tool engineering services," encompassing tool and machining condition selection for customers, as well as tool geometry development.[12] Section 4 provides a detailed description of concrete examples of these services.

3. Usage of and Points to Note about Chip Formation Simulation

3-1 Benefits and usage of chip formation simulation

Using workpiece and tool geometries and material properties along with cutting conditions as input information, the chip formation simulation analyzes elasto-plastic deformation and thermal conduction by means of numerical calculations, including FEM, and outputs information such as cutting resistance, chip geometry, and temperature and stress distribution. In contrast to physical cutting, chip formation simulation is, as with other numerical calculation-based simulations on the whole, advantageous in that (1) desired changes can be made in cutting conditions and material properties and (2) experimentally difficult-to-obtain information can be obtained with relative ease. Advantage (1) implies the computational potential of introducing physically impossible cutting conditions, e.g. cutting involving no friction. Advantage (2) includes the potential of obtaining difficult-to-experimentally-measure or troublesome-to-obtain information such as stress and strain with relative ease. Moreover, Advantage (2) refers to the potential of visualizing drilling and atomic-level machining, in which it is not possible to experimentally observe chip formation. These advantages are greatly beneficial in terms of academic research and are also highly useful from the perspective of industrial applications.

For tool development, chip formation simulation is primarily intended for use as a technique of evaluating tool design. Apart from that, chip formation simulation is quite beneficial in that, as in the case of using it for academic research purposes, it facilitates understanding of the fundamental mechanisms underlying the phenomena involved in cutting. For example, it is often the case that, after the occurrence of tool chipping, the tool is substantially damaged and what triggered the chipping or in what mechanism the chipping occurred is unclear by observing the tool conditions after cutting. In such cases, simulating similar cutting conditions will enable the user to look at stress values and surmise whether the chipping results from mechanical stress or not, and whether the cause is associated with a transient or steady state of the cutting process. Moreover, chip formation simulation provides educational benefits. Inexperienced engineers may not always be able to conceive phenomena that are comprehensible to experienced engineers. Theoretical and visual descriptions of such phenomena made possible by simulation facilitate understanding.

3-2 Points to note about simulation usage

While chip formation simulations are useful, several points should be noted before use, which are briefly explained below.

(1) Agreement between Experiment and Simulation

The issue of agreement between experimental and simulation results must always be addressed and checked when conducting a simulation. However, close examinations in this regard would be too much to retain the merits of simulation. A realistic and desirable method is to verify simulation results against relatively simple-to-obtain experimental data, such as of chips and cutting resistance, collected only under a few conditions, and, in cases of verified good agreement, to use simulations assuming adequate validity of other indicators of agreement. In this process, care should be taken specifically for the following two matters.

(1)-1 Chip Geometry

In the cutting process, the chip curls and forms in free space without being fully constrained by the tool. It is therefore difficult to simulate chip formation with more geometric accuracy than for other machining processes. There is no need to pay any attention to the usage of tool geometry and cutting conditions. However, to quantitatively determine the degree of agreement, in many cases, adjustments are made to the coefficient of friction across the interface between the chip and tool rake face that has a substantial effect on the curl of the chip.

(1)-2 Feed and Thrust Forces

Simulation results agree relatively well with experimental data for principal force, which is that part of cutting resistance applied perpendicularly with respect to the tool's rake angle. In contrast, simulated feed and thrust forces, which are orthogonal to the cutting force, tend to be smaller than experimental data. The reason is that, although in the region between the proximity to the cutting edge and the flank face, elastic recovery that pushes the tool has substantial effects on the feed and thrust forces, as shown in Fig. 3, divided elements tend to be insufficient in this small region, specifically in three-dimensional simulations. Consequently, for cutting resistance, it becomes necessary to evaluate the principal force alone or to evaluate the thrust force by a two-dimensional simulation that enables fine division of elements. Although most cutting processes are three-dimensional processes, in many cases of simulation, as in the aforementioned case, two-dimensional analyses are more effective than three-dimensional analyses.

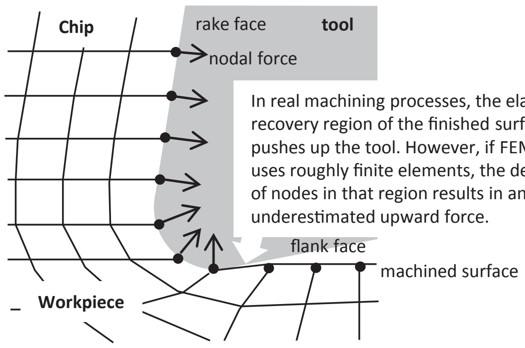


Fig. 3. Finite elements and nodal forces in region close to cutting edge

(2) Relationships between Simulation Results and Required Actual Properties

Chip formation simulation produces chip geometry, cutting resistance, temperature and stress data. It does not directly deliver data such as chip separation and tool life, though often needed in practical applications. It is therefore necessary to ascertain the relationships between the above data and actual properties desired for evaluation. For example, Ozaki et al.[13] developed a system to predict tool life by combining simulation and a model that describes tool wear.

(3) Combination of Chip Formation Simulation and Optimization Tools

Chip formation simulation is simply a method designed to estimate results under given conditions. To use it to design a tool, a scheme is additionally required to achieve optimization. In this light, taking required calculation time into account, a program that reduces the amount of calculation, such as combining simulation with the design of experiments, is also required. Moreover, in the case of three-dimensionally designed tools, identifying what parameters to optimize is of importance. In this regard, the designer's knowledge and insight are of service, as in conventional tool design.

4. Example Usage of Simulation

Adhering to the aforementioned concept, Sumitomo Electric makes optimal use of chip formation simulation, taking its characteristics into consideration. This section describes the following five cases as representative examples.

4-1 Fracture of high-feed turning inserts

The first case describes a simulation of insert fracture during turning conducted to investigate the causes of fracture and make certain which direction insert development should take. Figure 4 shows a distribution of the first principal stress depicted for turning with a general purpose chip breaker under a high-feed condition (f = 0.4 mm/rev). At this feed rate, inserts fractured on rare occasions initiating from the root of the chip breaker. Calculation results revealed tensile stresses applied in the root area, presumably causing fracture. We decided to change the geometry of the chip breaker root, explored stress-free geometry and applied it to physical turning. Thereafter fracture did not recur. Optimization made on the basis of this geometry led to the development of Sumitomo Electric's high-feed chip breaker family (Types SE, GE and ME).

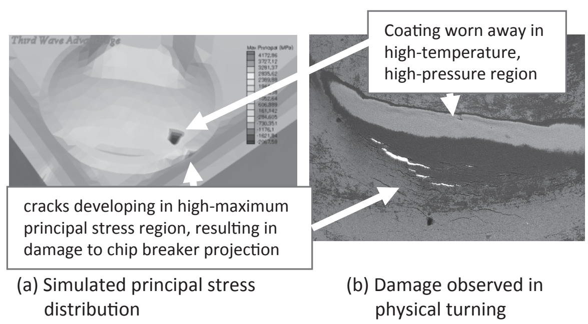


Fig. 4. Stresses applied to insert under high-feed condition and resulting damage
(SCM435, vc=200m/min, f=0.4mm/rev, ap=3mm)

4-2 Reducing burrs in face milling

This subsection describes an analysis case of the effects of the cutting edge geometry in association with burr formation in face milling. Figure 5 shows the corner geometry of the insert used on Sumitomo Electric's cutter Type DGC.(14) The general purpose insert Type G has rounded corner geometry, while Type FG designed to reduce burrs has chamfered corner geometry. Figure 6 shows analysis results for the state of workpiece deformation at the time of burr formation resulting from the use of these tools. A burr forms when a chip does not form cleanly along the path of the cutting edge and fails to leave the workpiece, i.e. when part of the chip remains on the workpiece. In comparison with Type G, Type FG produces higher strain at a location closer to the workpiece, within the stretched portion. More specifically, the stretched portion is separated at a location closer to the workpiece. As a consequence, smaller burrs remain on the workpiece.

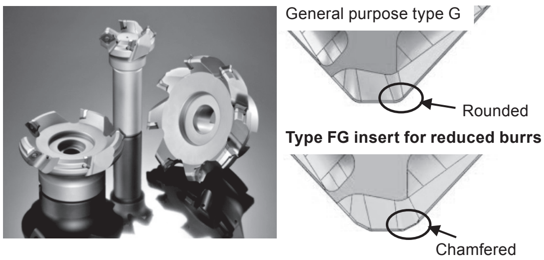


Fig. 5. Face milling cutter SEC-Dual Mill™ Type DGC

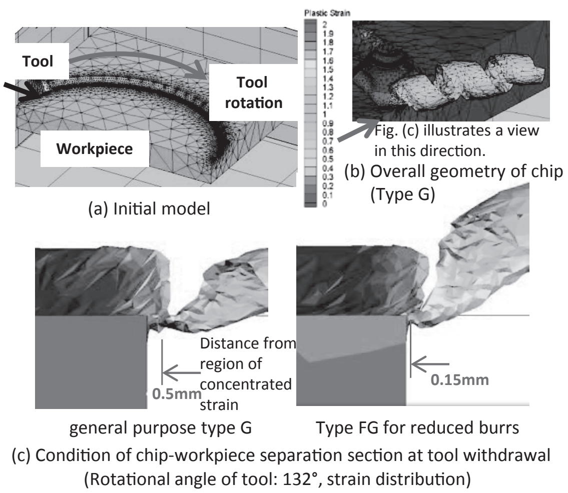


Fig. 6. Workpiece deformed upon tool withdrawal during face milling
(100 mm dia. cutter, SCM435, vc = 200 m/min, fz = 0.25 mm/t, ap = 2.5 mm)

4-3 Optimizing cutting edge specifications by combining simulation with design of experiments

Following the aforementioned usage of simulation intended to understand phenomena involved in cutting, this subsection presents an example of more direct use of simulation for tool design. This is a case of combination between two-dimensional simulation and the design of experiments. In this case, a simulation was conducted to design cutting edge specifications for cutting heat-resistant alloys. First, cutting edge specification parameters were selected. Using these parameters as factors in the design of experiments, an L18 orthogonal experiment*2 was conducted as an attempt to achieve optimization (Fig. 7). This process requires evaluation functions. Since simulation is unable to directly determine tool life, as discussed earlier, several factors, including cutting temperature, were chosen as factors influencing tool life. Using these factors as evaluation functions, we obtained several patterns of optimized tool geometry. Prototypes based on these patterns were physically constructed to evaluate their cutting performance. This process optimized tool geometry at the minimum amount of prototype tool construction and physical cutting evaluation.

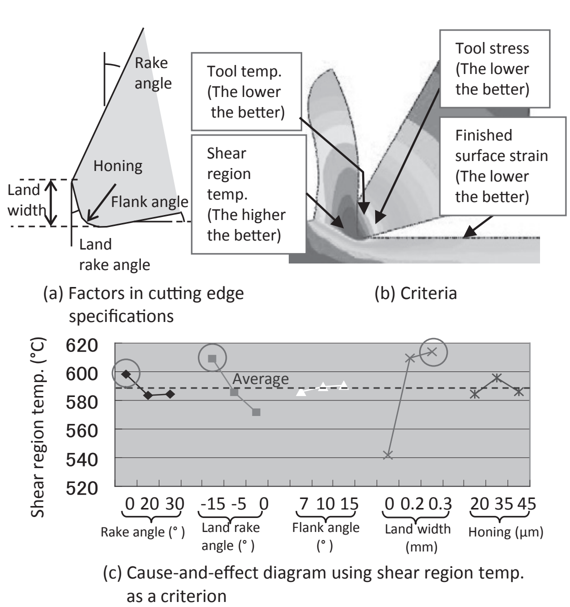


Fig. 7. Optimization of cutting edge specifications using design of experiments

4-4 Chip breaker design for grooving tools

This subsection describes an example of simulation applied to grooving tool design. In recent years, it has become common to provide grooving tools with three-dimensionally designed chip breaker geometry to improve chip treatment performance. Accordingly, three-dimensional simulation is used to design grooving tools. Figure 8 shows an example of analysis conducted for Sumitomo Electric's grooving tool Type GND.(15) This tool was designed specifically for improved chip treatment performance. However, as discussed earlier, it is difficult to directly evaluate chip separation by means of simulation. Therefore, for the evaluation, we used (1) chip curl diameter and (2) chip width as indicators. Three-dimensionally designed chip breakers are generally formed by stamping with a die. Simulation technology is highly effective in terms of reducing die fabrication cost and lead time.

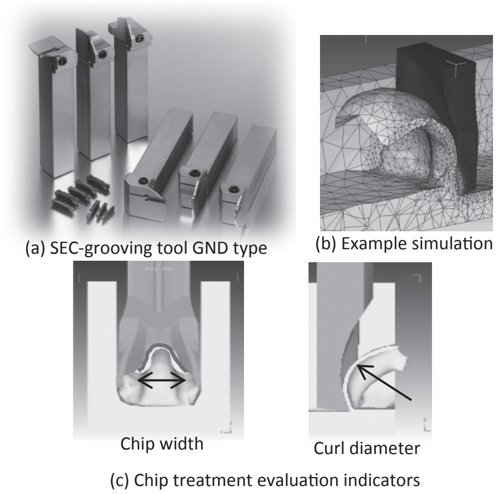


Fig. 8. Example analysis of grooving tools
(S13C, vc=150m/min, f=0.1mm/rev, edge width 3mm)

4-5 Evaluation of chip geometry formed by drilling into stainless steel

Lastly, this subsection presents an example of drilling analysis. Analysis of drilling processes is a high-computational-load type of three-dimensional simulation. However, the evolution of computational power and improved software are finally making this type of simulation feasible. Figure 9 evaluates the effects on chip geometry exerted by cutting edge geometry during drilling into stainless steel. In physical drilling, it is difficult to visualize how chips form in the region close to the cutting edge. In this respect, simulation is exceptionally effective. We have high expectations of this category, although at present simulation technology needs to be improved.

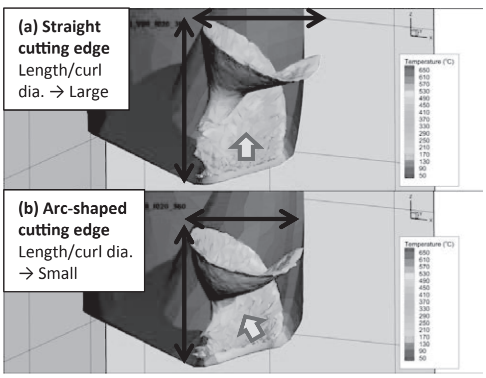


Fig. 9. Chip geometry forming during drilling into stainless steel
(8 mm dia. drill, SUS304, vc=80m/min, f=0.2mm/rev)

5. Conclusion

This report outlined the development process of chip formation simulation, providing explanations about example applications to tool development at Sumitomo Electric and about points to note on simulation usage. Chip formation simulation technology is still at an early stage of practical use. It still often fails to adequately reproduce phenomena and should be used with a thorough understanding of its characteristics. However, the potential of this technology is high. We intend to promote more effective use of chip formation simulation in the future.

Technical Terms

∗1 Finite element method (FEM): A numerical analysis technique; The finite element method is used to obtain an approximate solution of the overall behavior of the subject of analysis by dividing it into small elements and summing up calculation results for each element.

∗2 L18 orthogonal experiment: In the design of experiments, an orthogonal table is used to determine a set of factors. The L18 orthogonal experiment refers to the performance of an experiment using an orthogonal table that contains 18 patterns of seven factors of three levels and one factor of two levels (L18 orthogonal table). One feature of this experiment is that it is relatively free of factor-to-factor interactions.

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