Fast Switching SiC V-groove Trench MOSFETs

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High-efficiency power semiconductors are becoming increasingly important for an energy-saving society. While metal-oxide-semiconductor field effect transistors (MOSFETs) are basically made of silicon (Si), silicon carbide (SiC) MOSFETs have been finding commercial applications due to advantages such as high efficiency owing to their material properties. We have been developing SiC V-groove trench MOSFETs (VMOSFETs), which achieve high efficiency through the combination of SiC material properties and optimized trench structures. By introducing an electric field concentration layer into VMOSFETs, we have succeeded in suppressing a gate insulation film breakdown at the trench bottom and improved the breakdown voltage. Moreover, we have realized fast switching VMOSFETs with a reduced switching loss of up to 70% by optimizing the structures and reducing feedback capacitance.

Keywords: power device, 4H-SiC, trench MOSFET

1. Introduction

The modes of power generation and consumption have increasingly diversified on a global scale, as seen with the introduction of solar power and other renewable energy sources and the increased adoption of hybrid electric vehicles powered by high-capacity storage batteries. The technology designed to efficiently transmit and use generated energy is generally known as power electronics. Particularly, semiconductor power devices intended for power control applications are expected to serve as key energy-saving devices, reducing power conversion losses.

Most power devices are made of silicon (Si). Metal-oxide-semiconductor field effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs) are commonly used as power devices. Photovoltaic power conditioners and in-vehicle inverters for hybrid electric vehicles incorporate Si IGBTs. Using microfabrication techniques developed for large-scale integrated circuits, these power devices have improved in terms of loss and breakdown voltage. However, these characteristics have approached their theoretical limits calculated from properties such as breakdown electric field strength and saturated electron drift velocity. There is a growing demand for high-performance devices incorporating an innovative semiconductor material as an alternative to Si.

One major candidate material for innovative semiconductors is silicon carbide (SiC), which is a wide band gap semiconductor. Compared with Si, SiC features higher breakdown electric field, saturated electron drift velocity, and thermal conductivity. With these properties, SiC is excellent for power device applications. Intensive research and development is being conducted to produce power devices made of SiC to make optimal use of such properties to achieve a high-breakdown voltage, fast-operating, and low on-resistance device.[1] The first commercialized SiC device, which appeared in 2011, was a planar MOSFET forming a current controller (channel) in parallel with the semiconductor substrate surface. Compared with this, the trench MOSFET in which a channel is provided in a trench formed on the semiconductor substrate surface, is free of current constriction resistance. Consequently, enabling reduced resistance, the trench MOSFET is advantageous in reducing losses and is becoming the mainstream of SiC MOSFETs.

The SiC V-groove trench MOSFET (VMOSFET) under development at Sumitomo Electric Industries, Ltd. characteristically has a V-groove-shaped gate structure, the slanted trench walls of which are made up of $\{0\bar{3}3\bar{8}\}$ faces.[2],[3] As this crystal face has a higher channel mobility than other crystal faces, it is possible to reduce the channel resistance substantially. Consequently, the SiC VMOSFET outperforms previously developed MOSFETs in loss reduction. However, the SiC trench MOSFET needs to overcome a challenge that is latent with Si-based trench devices. This is that the gate oxide film at the trench bottom is liable to breakdown during high voltage application due to the occurrence of an electric field concentration because the breakdown electric field strength of SiC is 10 times higher than that of Si. By introducing a buried p-region as a field relaxing layer near the trench bottom, we relaxed the field of the oxide film otherwise intense at the trench bottom and worked on the development of a device that had both low-loss and high-breakdown voltage features. Furthermore, in addition to the use of smaller device design rules and structural optimization, the static capacitance of the MOSFET was reduced to achieve a device structure enabling fast switching. A buried p-grounded structure for electrically connecting the buried p-region to the source terminal and a process that would enable the buried p-grounded structure were also developed. Thus, we have realized a SiC VMOSFET capable of fast switching without compromising the low-loss and high-breakdown voltage features.

This paper reports on the SiC VMOSFET with buried p-grounded structure, focusing on its basic characteristics and, with inverter applications in mind, its switching characteristics.

2. Low-Capacitance Design Based on Buried p-Grounded Structure

A MOSFET is a device that has three terminals: gate, source, and drain. The gate voltage is used for on-off control of the MOSFET. When the gate is on, a large current can be passed between the source and the drain. Parasitic static capacitance is present between each pair of terminals, due to the structure of MOSFET. Switching operation necessarily involves a time taken to charge and discharge the capacitance, which greatly affects the switching rate.

The gate-drain capacitance C_{gd}, the gate-source capacitance C_{gs}, and the drain-source capacitance C_{ds} work as follows:

Input capacitance $C_{iss} = C_{gd} + C_{gs}$
Output capacitance $C_{oss} = C_{ds} + C_{gd}$
Feedback capacitance $C_{rss} = C_{gd}$

For fast switching of SiC VMOSFET and other high-breakdown voltage devices, it is particularly important to reduce the feedback capacitance C_{rss}. The newly developed MOSFET has a buried p-region connected to the source terminal via a p-layer to reduce C_{rss} and improve the switching time.

Figure 1 presents schematic cross-sectional diagrams of the SiC VMOSFET and illustrates the C_{rss} components. Figure 1 (a) shows the conventional structure, in which the buried p-region is not grounded to the source terminal. Figure 1 (b) shows the newly developed structure reported in this paper, in which the buried p-region is grounded to the source terminal via the p-connecting region. Hereinafter, the structures illustrated in Fig. 1 (a) and (b) are referred to as the floating structure and the grounded structure, respectively. In Fig. 1, in addition to the structures, individual capacitance components that affect C_{rss} are indicated. The floating structure shown in Fig. 1 (a) has C_{rss}, as expressed below.

$$C_{rss} = C_{gd} = C1 + (C2^{-1} + C3^{-1})^{-1}$$

Meanwhile, because the buried p-region is grounded to the p-layer of the source C_{rss} of the grounded structure illustrated in Fig. 1 (b) is expressed, as follows:

$$C_{rss} = C_{gd} = C1$$

Thus, C_{rss} is reduced by the amount of capacitance attributable to the buried p-region. Since the buried p-region is connected to the source terminal, capacitances $C2$ and $C3$ are converted to C_{ds} and C_{gs} and no longer affect C_{rss}.

In addition to the above, the newly developed MOSFET employs finer design rules and has an optimized basic structure, including the dimensions of the buried p-region, with C_{rss} reduction in mind.

3. Fabrication Process

The grounded structure presented in Fig. 1 (b) was fabricated in the following process, which is detailed in Fig. 2. The first epitaxial layer was grown on an n-type 4° off 4H-SiC (000$\bar{1}$) substrate. In the first epitaxial layer, a buried p-region was formed by aluminum (Al) ion implantation [Fig. 2 (a)]. Next, a 1-µm thick second epitaxial layer was grown. Similarly, in the second epitaxial layer, a p-connecting region intended to electrically connect the buried p-region to the upper p-region of the source was formed by Al ion implantation [Fig. 2 (b)]. Additionally, a 1-µm thick third epitaxial layer was formed. The p-region of the source and the buried p-region were grounded by forming, in the third epitaxial layer, p+ and p-body regions as the p-region of the source. An n+ region necessary for current passage was formed in the third drift layer by phosphorus (P) ion implantation [Fig. 2 (c)]. Separate two-layer formation of the second and third epitaxial layers made it

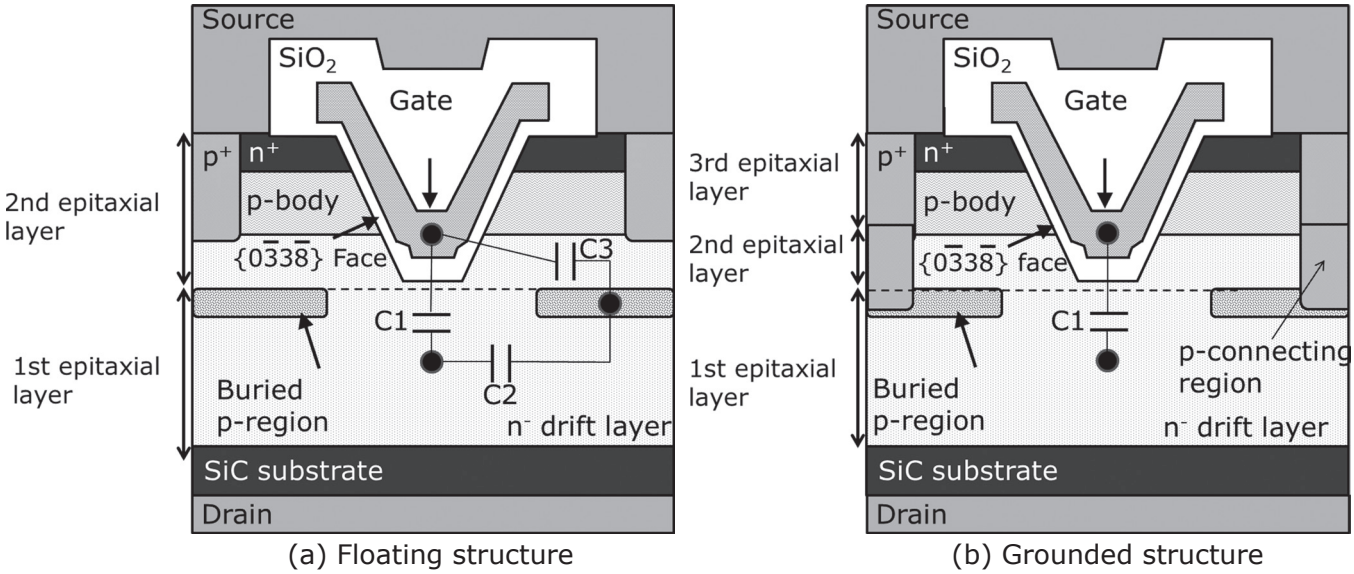

Fig. 1. Schematic cross-sectional diagram of SiC VMOSFET and C_{rss} components

possible to fabricate the grounded structure with a typical ion implanter rated in the hundreds of keV class.

We formed the V-groove trench structure by growing {0$\bar{3}\bar{3}$8} crystal faces on the trench side walls through a thermochemical etching process in a chlorine (Cl_2) atmosphere, using a thermally oxidized film as an etching mask.[4] In this process, the channel length of the trench sidewalls was 0.6 µm. Figure 3 shows a scanning electron microscope (SEM) image of a formed trench. The formed trench structure is favorable as revealed by the smooth sidewalls of the trench.

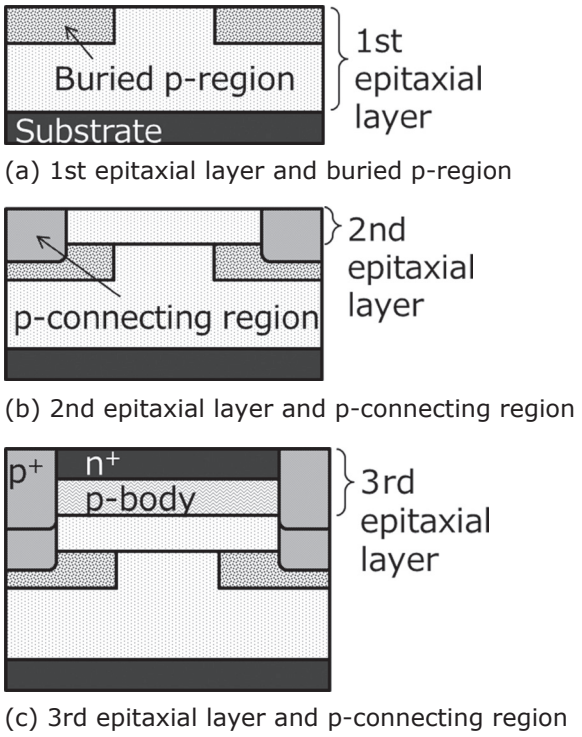

Fig. 2. Fabrication process for SiC VMOSFET

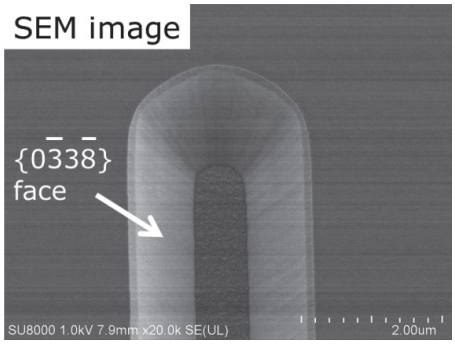

Fig. 3. SEM image of a formed trench

The gate oxide film was formed by thermal oxidation of SiC. After oxidation, nitriding of the interface of the oxide film was performed using nitrogen monoxide to reduce defects occurring at the interface between SiC and the oxide film. The final thickness of the oxide film of the gate was 50 nm, except for the trench bottom where the film was 200 nm thick. Polycrystalline silicon was used to form the gate terminal. The chemical vapor deposition (CVD) process was used to grow SiO_2 to cover the gate terminal. After opening an aperture in SiO_2 in the source terminal area, nickel (Ni) films were formed by sputtering as ohmic source and drain terminals. Alloying heat treatment was performed at a temperature enabling reaction between SiC and Ni. Subsequently, an Al pad was formed over the terminals to complete the structure illustrated in Fig. 1 (b).

4. Characteristic Evaluation

4-1 Capacitance characteristics

The SiC VMOSFET used in the experiment was 3 mm by 3 mm in chip size. Figure 4 shows C_{rss} measurements in relation to the drain-source voltage (V_{ds}) of grounded and floating structures. Under the condition of V_{ds} = 300 V, C_{rss} of the grounded structure was 10 pF, roughly a half of C_{rss} of the floating structure (19 pF). This is the capacitance reduction effect achieved by grounding the buried p-region, as illustrated in Fig. 1.

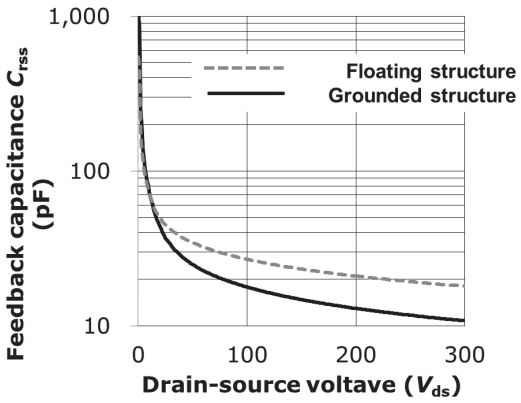

Fig. 4. Capacitance characteristics of SiC VMOSFET

4-2 Switching characteristics

Switching characteristics were measured with the switching circuit shown in Fig. 5, encapsulating the

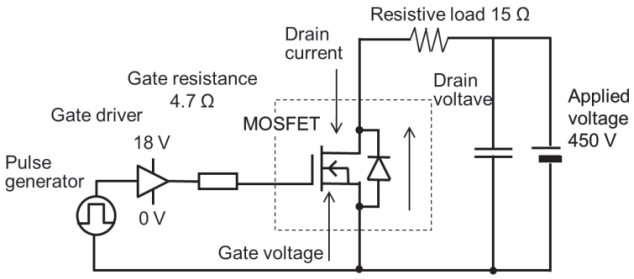

Fig. 5. Switching circuit

MOSFET in a TO-247 package. The applied voltage was 450 V, the resistive load was 15 Ω, and the external gate resistance was 4.7 Ω.

Figures 6 and 7 compare the turn-on and turn-off switching waveforms of the grounded and floating structures, respectively. As shown in Table 1, typical rise time (t_r) and fall time (t_f) were t_r = 40 ns and t_f = 14 ns for the floating structure, and t_r = 24 ns and t_f = 16 ns for the grounded structure. Switching involves energy loss. The turn-on loss (E_{on}) and the turn-off loss (E_{off}) were: E_{on} = 97 μJ and E_{off} = 55 μJ for the floating structure, with the total switching loss reaching 152 μJ, and E_{on} = 62 μJ and E_{off} = 66 μJ for the grounded structure, with the total switching loss reaching 128 μJ. Consequently, the total switching loss was reduced by approximately 16%.

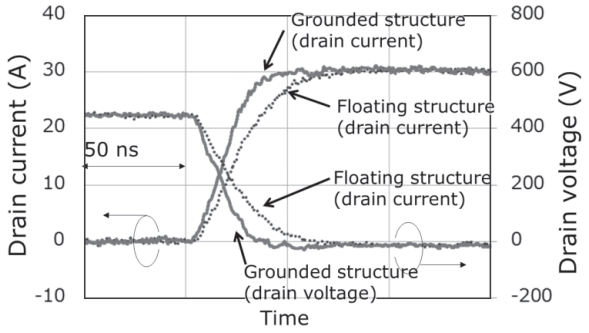

Fig. 6. Turn-on switching waveforms

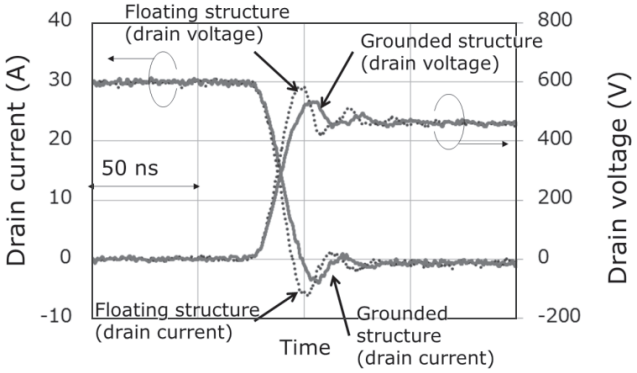

Fig. 7. Turn-off switching waveforms

Table 1. Switching characteristics of SiC VMOSFET

	Floating structure	Grounded structure
t_r [ns]	40	24
t_f [ns]	14	16
E_{on} [μJ]	97	62
E_{off} [μJ]	55	66
Total switching loss [μJ]	152	128

The above results revealed that C_{rss} reduction is effective for reducing t_r and concomitant E_{on}. Meanwhile, the C_{rss} reduction did not affect the falling rate. This means that the parasitic inductance of the source was rate-determining, generating an induced electromotive force in the opposite direction to the behavior of turning off the gate.

The total switching loss of the previously developed MOSFET[5] before structural optimization was 416 μJ. Accordingly, the newly developed MOSFET has a switching loss cut by approximately 70%, including reduction attributable to improved basic characteristics achieved by structural optimization.

5. Future Developments

Power devices rated in the medium breakdown voltage range from hundreds of V to 1,700 V are used in a wide range of applications, including photovoltaic power conditioners, hybrid electric vehicles, and industrial motor inverters. The size of the market for such power devices is correspondingly large. In the market, Si IGBT power devices are currently predominant. To achieve the goal for the newly developed MOSFET, which is to replace Si IGBT power devices with SiC devices, the challenge is to reduce the cost to a similar level to that of Si devices. As SiC substrates are expensive, chip size reduction enabled by resistance reduction will lead to improved cost competitiveness. In this respect, with its potential to enable resistance reduction, the VMOSFET has an advantageous structure. Furthermore, switching rate improvement, as provided by the newly developed structure, makes it possible to raise the system frequency. This implies the possibility of reducing the sizes and weights of inductors and capacitors, thereby paving the way to the size and cost reduction of the overall system.

6. Conclusion

To make V-groove trench MOSFETs (VMOSFETs) formed on 4H-SiC (000$\bar{1}$) fast-switching, we designed a buried p-grounded structure for reducing C_{rss} and developed a process that would realize the design. The results of characteristic evaluation revealed that C_{rss} decreased by half, as intended, the rising rate decreased from 40 ns to 24 ns, and the total switching loss was reduced by 16%.

Moreover, including the effects of structural optimization, the newly developed MOSFET had a total switching loss approximately 70% lower than the previously developed MOSFET.

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