High-Quality 6-inch SiC Epitaxial Wafer “EpiEra”

Keiji WADA*, Takemi TERAO, Takaya MIYASE, Tsutomu HORI, Hideyuki DOI, and Masaki FURUMAI

Power devices have been essential to significantly advance efficient electric power use mainly for a future electric network society that will use versatile energy sources such as renewable energy resources and electric vehicles. SiC power devices are expected to be a key for power conversion systems to cut back electric power loss. To achieve large chip dies used in high current ratings, the wafer size of SiC substrates has increased, requiring precisely controlled fabrication processes. The epitaxial layer used for the drift region in a device structure strongly influences the device performance, entailing to the requirement of epitaxial defects reduction as well as the precise control of doping concentration and thickness for stable chip production. We have successfully demonstrated an extensive defect-free epitaxial layer with an excellent doping concentration and thickness uniformity on a 150-mm diameter 4H-SiC substrate.

Keywords: silicon carbide, power devices, epitaxial growth

1. Introduction

Usage of renewable energy, such as solar and wind power, is expanding to lower fossil fuel consumption and thereby reduce production of greenhouse gases. At the same time, storage batteries and electric vehicles are becoming widespread among households and business sites. Also, the modes of power usage—from generation to consumption—are diversifying, such as by networking the power grid to balance supply and demand through advanced monitoring systems.

Power semiconductor devices are used for electric energy transformation from one form to another, which occurs a number of times in the processes of power generation, supply, and consumption. Replacement of such power semiconductor devices, which commonly use silicon (Si) semiconductors at the moment, by more efficient silicon carbide (SiC) power devices is progressing towards improving power usage efficiency.[1]

In recent years, power modules using SiC power devices that offer relatively high current capacities of more than 100 A are becoming available in the market. This encourages expectations of the application of SiC devices to power electronic equipment to reduce power loss. At the same time, the diameter of SiC wafers is increasing. A 6-inch wafer has been commercialized, and the size of dies is being enlarged to produce a high current device. For this reason, demand for quality improvements in SiC materials is also increasing in terms of performance stability and reliability. It is the SiC epitaxial layer that determines performance uniformity and the yield of transistors and diodes formed on the wafer. It is important that the thickness and doping concentration of the epitaxial layer grown on the SiC wafer are uniform, because they influence the distribution of device’s blocking voltage and on-state characteristics on the wafer. Typically, SiC epitaxial growth is carried out through chemical vapor deposition (CVD) in a high temperature environment of 1,500°C or higher.[2] As this temperature is higher than the Si melting point, SiC epitaxial growth technology has a shorter history of R&D compared to that of the Si semiconductor production technology. Thus, it is considered that there are issues to address concerning heat distribution at a high temperature and production process stabilization for multiple or large wafers. For example, epitaxial defects, such as down-falls and triangular-defects as shown in Fig. 1, may appear on the surface of the SiC epitaxial layer during epitaxial growth.[1] As such defects cause significant deterioration in device performance, known as a “device killer defect,” and it is therefore important to minimize such defect density. Note that a SiC substrate produced by sublimation growth, which is commonly used, usually contains several hundred to several thousand cm^{-2} of threading edge dislocations (TEDs), threading screw dislocations (TSDs), basal plane dislocations (BPDs), as well as other combined dislocations. Out of these dislocations, when a BPD in the substrate propagates into the epitaxial layer, the BPD causes the expansion of stacking fault due to the minority carrier recombination while the bipolar current is applied, deteriorating the reliability of devices.[3] For this reason, the BPDs in the substrates are converted to TEDs, which are generally regarded to be harmless during the epitaxial growth.[4] Sumitomo Electric Industries, Ltd. has achieved a reduction in the above crystallization faults, while maintaining quality including highly uniform doping concentration and thickness of the epitaxial layer grown on multiple 6-inch wafers through CVD.

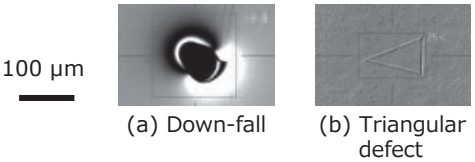

Fig. 1. SiC epitaxial defects

2. Epitaxial Growth of SiC by CVD

2-1 Hot-wall CVD for SiC epitaxial growth

A SiC epitaxial layer was formed using a hot-wall CVD reactor that can make it grow on multiple 6-inch wafers simultaneously. Figure 2 is a schematic structure of the hot-wall CVD reactor. Within the quartz chamber, there is a graphite susceptor that is heated by a high frequency induction heater and this susceptor is surrounded by thermal insulators. SiC wafers are placed on a rotating susceptor plate. The growth temperature is about 1650°C, and silane (SiH_4) and propane (C_3H_8) are used as precursors. The epitaxial layer was grown through low pressure CVD, in which hydrogen was supplied as a carrier gas and decompression is carried out by dry-pump exhaust.

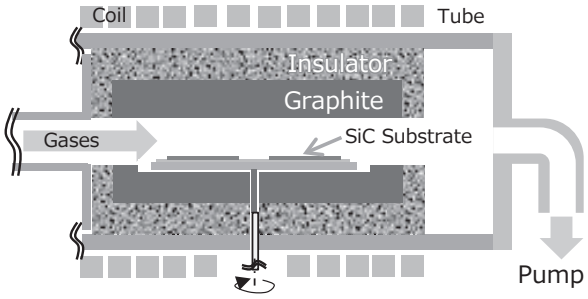

Fig. 2. Schematic structure of hot-wall CVD

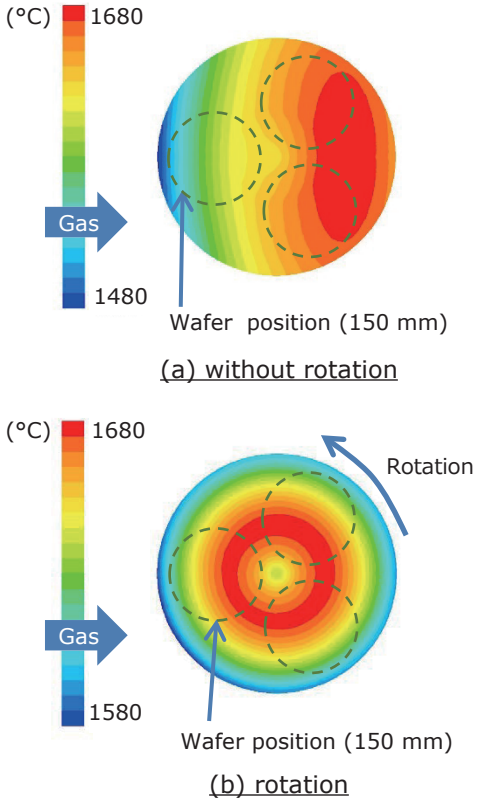

Fig. 3. Temperature distribution by Simulation analyses

2-2 Characterization to SiC epitaxial layer

The thickness of the SiC epitaxial layer was measured by interference spectra analysis using Fourier transform infrared spectroscopy (FTIR). On the other hand, the doping concentration was estimated by capacitance-voltage (CV) measurement. Defects on the surface of the epitaxial layer were observed and counted automatically using confocal optical microscopy with a stage scanner. Propagated BPDs from the substrates into the epitaxial layer were observed by photoluminescence (PL) imaging at room temperature.

3. Temperature Distribution Analyses by Numerical Simulation

The temperature distribution of the area where the 6-inch wafers are placed was studied by thermofluid simulation. Figure 3 shows the temperature distribution of the rotating susceptor on which the 6-inch wafers were placed. The susceptor is normally rotating during epitaxial growth. The result (a) is the temperature distribution simulation if the susceptor is not rotated, and (b) is the temperature distribution while the susceptor is rotated.

As can be seen in (a), the upstream region where the source gases are supplied shows a lower temperature as it is cooled mainly by the hydrogen carrier gas. Rotation of the susceptor reduces the temperature difference on its surface, however, the lower temperature tendency remains on the outer edge of the susceptor. Also, the center of the susceptor shows a lower temperature, possibly due to heat removal via the rotating rod.

4. High-Quality SiC Epitaxial Wafer "EpiEra"

4-1 99% killer defect free high-quality SiC epitaxial layer

We assessed BPDs in the epitaxial layer using PL imaging. BPDs in the substrates generated during sublimation growth are thought to derive from thermal stress.[5] The BPD density contained in the 6-inch SiC wafer we used in this developments was from approximately 1000 cm^{-2} to 3000 cm^{-2}. In general, BPDs appearing on the wafer surface tend to affect the growth direction in which the image force of dislocation is reduced during epitaxial growth. Thus, most BPDs are converted to TEDs during the growth. However, not all BPDs are converted to TEDs, depending on the epitaxial growth conditions.[6] Figure 4 (a) shows the BPD distribution on the surface counted using PL imaging for the epitaxial layer grown under the conventional conditions. In the case when BPDs are easily propagated into the epitaxial layer, the BPD density within the layer shows a high value of 20 cm^{-2} or more. A comparison with the temperature distribution, as shown in Fig. 3, also indicates that the propagated areas are highly correlated with the high temperature zones on the wafer. It is assumed that the BPDs are generated under thermal stress during growth, in the same way as in the wafer formation through sublimation growth. However, we managed to reduce the BPD density in the epitaxial layer to 0.1 cm^{-2} or less, as shown

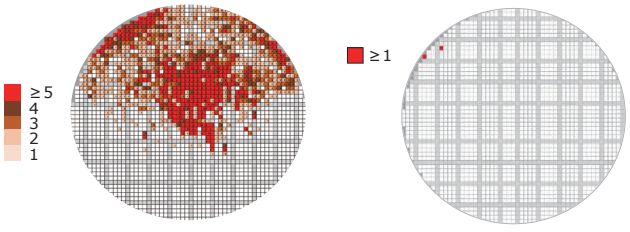

Fig. 4. BPDs count maps of SiC epitaxial layer

in Fig. 4 (b), through improving the growth drive that predominantly converts BPDs to TEDs by introducing a buffer layer in the early stages of growth. In this case, a defect-free area (DFA) where there are no BPDs within a wafer area sectioned by a 2.6 × 2.6 mm^2 PL imaging view showed an extremely high ratio of 99.9%.

In the same manner, we were able to significantly reduce the appearance of killer defects through optimizing the growth process and reactor environment. As mentioned earlier, SiC epitaxial growth carried out under a high temperature environment could be associated with defects, for example, generation of byproducts such as polycrystalline SiC during the early stages of the degradative reaction of the material gas, down fall of such byproducts and other foreign particles, and triangular defects that internally contain stacking faults. To avoid foreign particle fall down and accumulation on the wafer, we cleaned the interior of the reactor. We also stabilized and optimized the epitaxial surface growth at its beginning, i.e. when introducing the material gas. Through these improvements, we could reduce defects other than BPDs to a level equivalent to the value of the BPD density or less. The average value of fall down defect in the killer defect map was 0.05 cm^{-2}, and that of triangular defects was 0.08 cm^{-2}. Figure 5 shows the defect map of the reduced killer defects on the epitaxial layer.

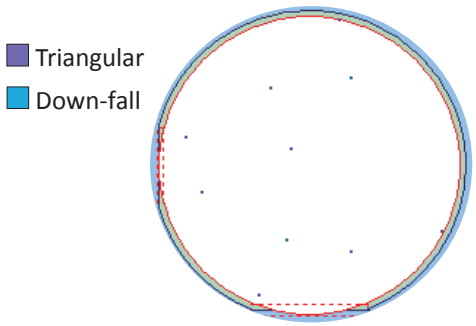

Fig. 5. Epitxial defects distribution on the SiC epitaxial layer

4-2 Stability of epitaxial defects reduction in the improved epitaxial growth

Figure 6 represents a normal distribution plot of the defect density over 20 epitaxial layers grown on 6-inch wafers, which was obtained to evaluate the epitaxial growth process with lower BPDs and less device killer defects. The average number of any of the defects over 20 layers is less than 0.1 cm^{-2}, suggesting quite stable growth. In the same way, the average value of the BPD density was 0.1 cm^{-2}.

The total number of defects and their distribution affect the performance distribution and yield depending on the die size of the SiC power device built on the epitaxial layer. In a typical epitaxial layer as evaluated in this paper, for example, an area sectioned by 2 × 2 mm^2 was 99% defect free, which is converted to a high value of 98% for a 5 × 5 mm^2 area.

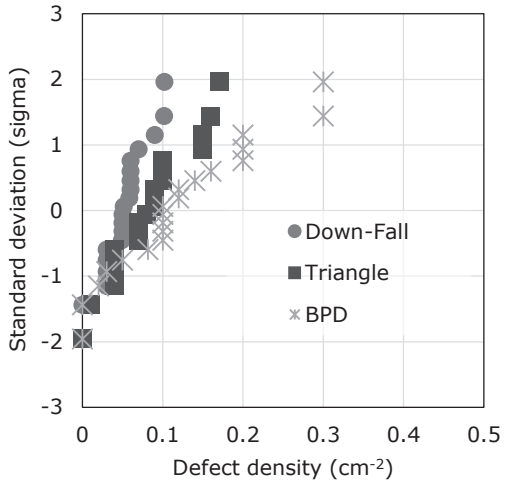

Fig. 6. Stability of epitaxial reduction in improved CVD growth

4-3 Doping and thickness uniformity of the SiC epitaxial layer

Due to the influence on characteristic distribution of the device's blocking voltage and on-state resistance, the layer thickness and doping concentration of the epitaxial layer formed on the SiC wafer are required to be highly uniform across its whole surface. The outer periphery of the wafer is generally on the border of the rotating disk, hence the temperature variation and changes in gas reaction to such variable temperatures are large, which can in particular cause variable doping concentration.[5] Sumitomo Electric has been developing its own exclusive epitaxial growth process by analyzing the gas temperature distribution during the growing process based on simulation analysis results. We designed and manufactured an epitaxial layer of 10 µm thickness and 8 × 10^{15} cm^{-3} doping density on a 6-inch wafer. Figure 7 shows the thickness distribution over 41 points on the layer surface, and Fig. 8 shows the doping distribution. The average thickness was 10.1 µm within a range of 9.9 to 10.6 µm, exhibiting extremely high uniformity. The σ / average was 1.9%. As for the doping uniformity, the average value was 8.1 × 10^{15} cm^{-3}, and remained in a range of 7.6 × 10^{15} to 8.4 × 10^{15} cm^{-3}. We obtained 2.2% as the σ / average, which is an extremely high density uniformity value for layers grown on multiple 6-inch

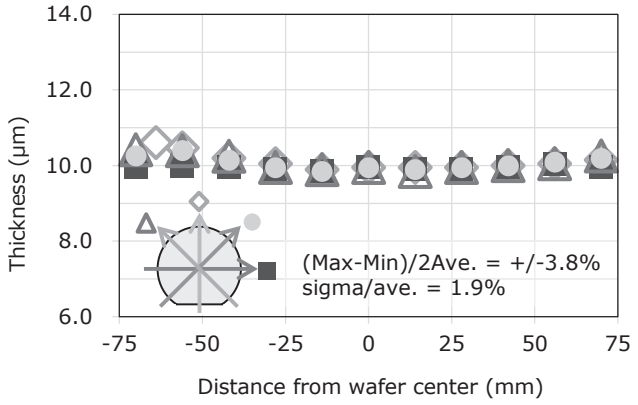

Fig. 7. Thickness uniformity of the SiC epitaxial layer

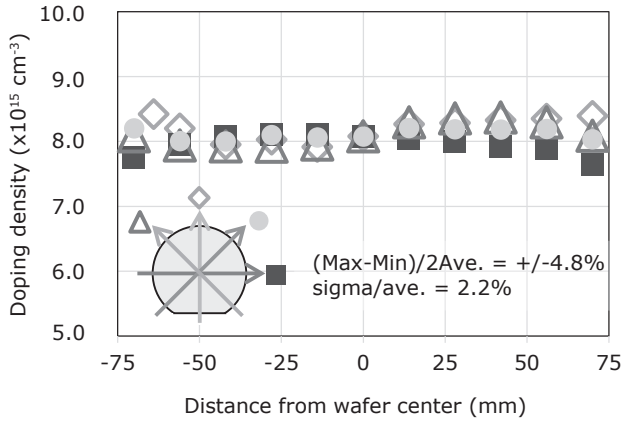

Fig. 8. Doping concentration uniformity of the SiC epitaxial layer wafers.[7],[8]

5. Conclusion

We conducted the epitaxial growth utilizing a hot-wall CVD reactor that can grow SiC epitaxial layers on multiple 6-inch wafers. We found that it was possible to convert almost most BPDs contained in the wafer into TEDs by optimizing the grouth condition of buffer layer growth. We could also demonstrate that stable reduction of epitaxial killer defects, which are highly influential on device performance, can increase the defect-free areas on the epitaxial layer. Along with these improvements, we obtained high uniformity in the epitaxial layer thickness and doping concentration, which contributes to the characteristic uniformity of devices fabricated on the epitaxial layer. We believe that our achievement will significantly contribute to enlarging the die size and improving the reliability of SiC devices towards realizing a higher current capacity in such devices.

References

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